Scalable Power Electronics Architecture with Multiplex Switching and Coupled Magnetics

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Abstract

Power electronics are a driving force for the electrification of society, including transportation, communication and computing systems, and the modern power grid. High-performance applications, contemporary and future, will constantly demand greater efficiency, speed, and density; to power these scalable loads, power electronics must also be scalable. However, existing analysis frameworks lack the rigor and generality needed to understand scalable power converters across different applications, operating conditions, and technologies. Moreover, scaling up power converters exponentially increases the design, balancing, and control complexity. This thesis addresses these challenges by presenting a general design method for a scalable power electronics architecture; envisioned in this method are a family of topologies leveraging multiplex switching and coupled magnetics to readily scale to the demands of future high-performance loads.

First, this thesis develops a general mathematical framework for the balancing of scalable power converters combining multiplex switching and coupled magnetics; this framework proves that coupled magnetics passively balance multiplex switches agnostic of the operating conditions. This technique is experimentally demonstrated as a scalable alternative to the limited applicability and effectiveness of existing methods. Second, this thesis demystifies and demonstrates the multi-resonant internal dynamics of scalable power converters with many coupled switches and passives, yielding design guidelines for dynamically stable scalable converters. Next, this thesis leverages these new theories to design a converter with 128 multiplex switches, an order-of-magnitude increase from existing work. 60 flying capacitors are balanced with one four-phase coupled inductor, allowing a 64$\times$ multiplication of the switching frequency and unlocking the regime of above-switching-frequency modulation. Finally, this thesis defines a scalable power architecture with wide applicability in communication-over-power applications; it is demonstrated with a four-phase, seven-level light fidelity (Li-Fi) transmitter achieving state-of-the-art performance: 95.8% efficient, 1000 W illumination and 6.4 Mbps communication over 20 m.

Acknowledgments

To be written.

To my family.

"Let us remember always how good it was here, when we were all together, united by a good and kind feeling which made us … better perhaps than we are in everyday life." — Dostoevsky

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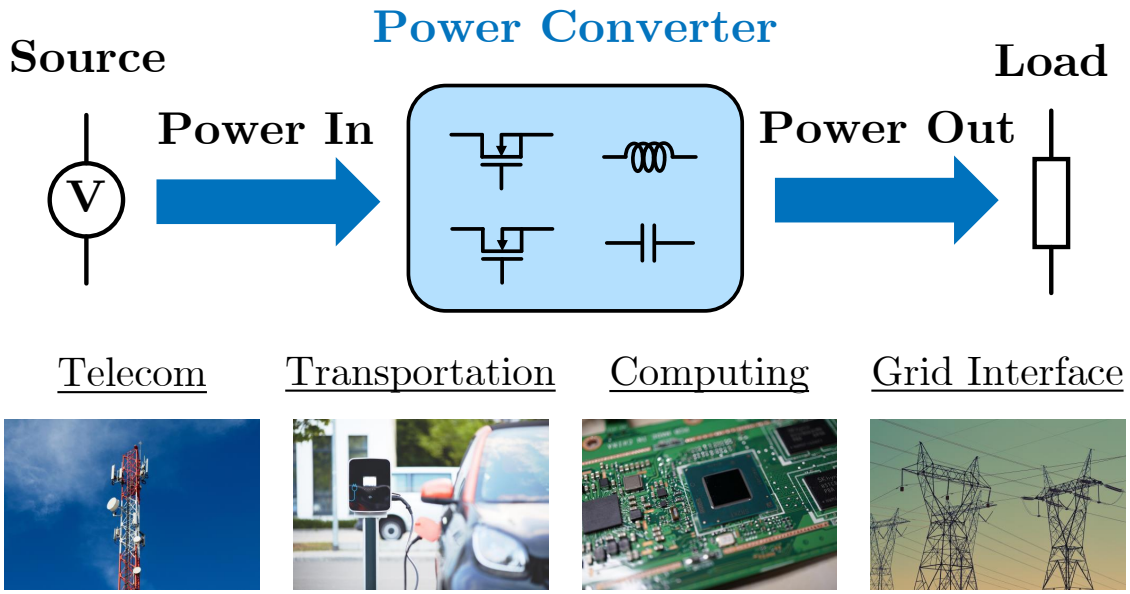


Figure 1.1: Power electronic converters, at their core, convert power in one form from a source to another form that is useful for powering a load. This can be accomplished with switches, inductors, and capacitors. Bottom images provided courtesy of [1–4].

1.1 Scalable Power Electronics for High-Performance Loads

Power electronics are critical for enabling and accelerating the continued electrification of modern society. As such, advancing the performance of power electronics can unlock new capabilities for the most fundamental human activities, including communication, computing, transportation, and power generation, storage, and distribution. Advanced power electronics have made a key impact in numerous high-impact technologies by, for example: (i) forming the backbone supplying the massive surge in AI and data center power consumption [6–11], (ii) powering 5G power amplifiers and a wealth of emerging communication technologies [12–14], (iii) advancing cutting-edge semiconductor manufacturing with nanosecond-scale control of complex plasma loads [15, 16], (iv) developing a more robust, efficient, and clean electric grid [17], and (v) driving transportation electrification forward with high-efficiency motor drives [18].

The core principles and goals of power electronic converters are simple (Fig. 1.1). Electrical power from a source (e.g. grid, battery, solar panel) is converted from one form (particular voltage, current, frequency, etc.) to another, in order to power a load. Most modern power converters accomplish this with a combination of switches, inductors, and capacitors, which allows the

process to be completed (theoretically) without loss. Many power conversion processes, such as voltage step-up and step-down, can be completed with just two switches, one inductor, and one capacitor [19]; for example, the "buck", or step-down, converter in Fig. 1.2 steps a higher input voltage V_{in} down to a lower output voltage v_{out} used to power a load Z_{o}. This is accomplished by repeatedly toggling two complementary switches at a high switching frequency f_{sw} to "sample" the input voltage at the "switch node" v_{sw} with some duty cycle d between 0 and 1. The switch node is filtered with a power inductor L and capacitor C_{o} to extract the dc component that is used to power the load.

The buck converter is the simplest "canonical" cell completing the step-down operation [19] with only two switches and a filter. While simple canonical converters are robust, predictable, and easy to design, they are wholly insufficient for powering the emerging high-performance loads previously mentioned. Fundamentally, these converters suffer from a lack of scalability; they cannot be extended to provide the power level, efficiency, response speed, modularity, or density required by increasing complex and large-scale loads.

Take, for example, the intrinsic trade-off between the efficiency and response speed of the buck converter in Fig. 1.2: in order to improve the response speed to sudden load changes (e.g. burst of CPU activity), the converter must be switched at a higher frequency f_{sw}. Doing so allows the use of smaller passive components, since the inductor current ripple $\Delta i_L \propto \frac{1}{f_{\text{sw}}}$ and output capacitor voltage ripple $\Delta v_{Co} \propto \frac{1}{f_{\text{sw}}}$ are both inversely proportional to operating frequency [19]. Smaller passive components means a higher cut-off frequency, $f_{LCo} = \frac{1}{2\pi\sqrt{LC_o}}$, allowing for higher control bandwidth and faster response speed. However, increasing the switching frequency also increases switching losses; energy is lost every time a switch is toggled, due to current and voltage overlap and parasitics such as the switch capacitances (e.g. C_{ds} in Fig. 1.2) [19, 20]. These switching losses, $P_{\text{switching}} \propto f_{\text{sw}}$, are proportional to the operating frequency, and reduce the converter's efficiency. Therefore, the efficiency and response speed of the buck converter are a conjugate pair traded off by one variable, the switching frequency. A simple converter like this is not scalable; optimized to a given technology (switches, passives, interconnects, packaging,

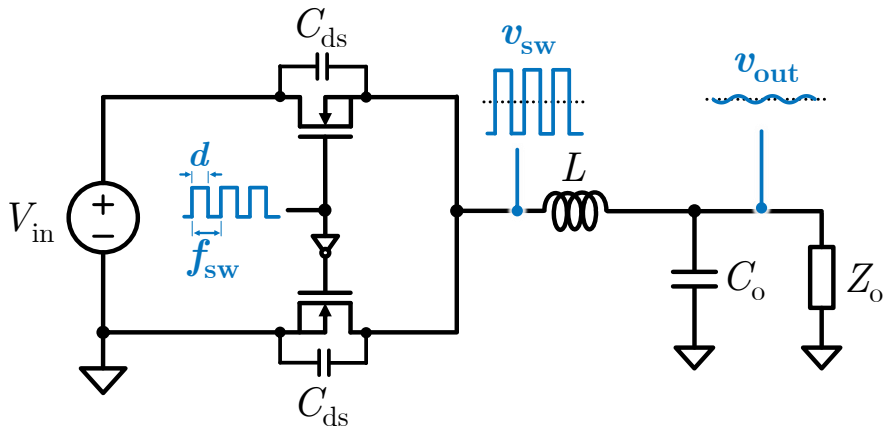


Figure 1.2: Key components and operating principles of a synchronous (two active switch) "buck", or step-down converter.

etc.), the efficiency and speed cannot be improved without sacrificing the other. In simple terms, we want the efficiency of a converter switching at 50 kHz, but want the response speed of a converter switching at 5 MHz; the question is, how do we achieve both?

To resolve the efficiency-speed tradeoff, among others, we must turn to more advanced power topologies. For example, the step-down function can be performed with (i) multiple buck converters extended in parallel to share the load current [21], (ii) multiple switches stacked in series with a phase shift to form multi-level converters with improved switch node resolution [22], and (iii) multiple stages of power conversion that decouple low frequency, high-efficiency stages from high-frequency, fast-response stages [10, 23, 24]. Passive components can also be improved, for example, by (i) replacing inductor volume with capacitors, which have higher energy density and scale better to smaller volumes [25], or (ii) combining multiple parallel inductors into coupled inductor structures that reduce size, ripple, and response time [5, 26–29]. All of these methods (multiphase, multilevel, and multistage switching, coupled inductors, hybrid switched-capacitors...) belong to a family of techniques that compose scalable power architectures (Fig 1.1). This thesis focuses in particular on two fundamental techniques encompassing the above: multiplex switching (relating to the active devices) and coupled magnetics (relating to the passive devices), and especially focuses on how both these scalable techniques enable fundamental improvements to the efficiency and speed of a power converter. The proceeding two

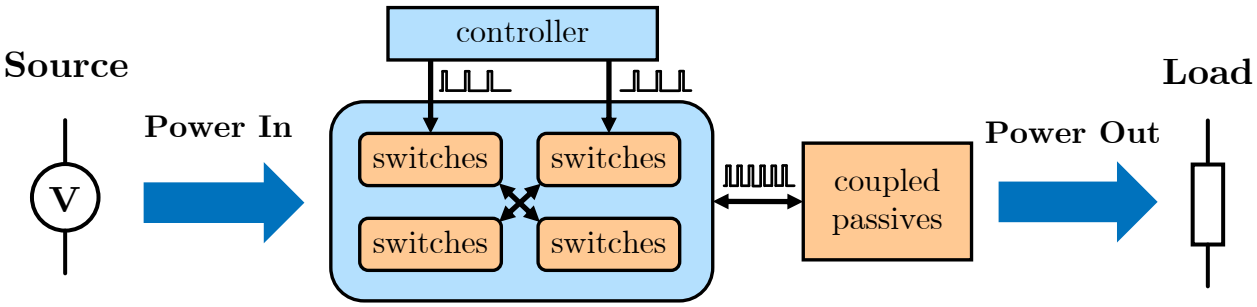


Figure 1.3: Diagram of a scalable power architecture leveraging multiplex, interleaved switches and combined, coupled passives. This thesis shows how the combination of these two techniques enables balanced, robust frequency multiplication which is readily scaled, fundamentally improving the efficiency-speed tradeoff limiting traditional converter topologies.

subsections introduce the existing background on multiplex switching and coupled passives and the knowledge gaps addressed by this thesis.

1.1.1 Background on Multiplex Switching and Frequency Multiplication

Although most power conversion processes can be completed with two switching devices, it is often beneficial to use more. Switches can either be placed in parallel to divide the on-state current, or in series, to divide the off-state blocking voltage; together, these techniques are forms of "multiplex switching" and form multiphase [21] and multilevel [22, 30] converters respectively. The fundamental benefit of multiplex switching is gaining the ability to control the switches with independent control signals; by properly phase shifting the switching actions, one can multiply the effective switching frequency seen by the output and energy storage components without increasing the switching frequency (or associated switching loss) of the individual switches.

This principle is illustrated in Fig. 1.4, which compares a two-switch buck converter to a two-phase, three-level flying capacitor multilevel (FCML) converter with eight interleaved switches. The converter is called two-phase because there are two parallel converters, each with an inductor L, sharing the load current I_o, and three-level because there are two series-stacked switches per phase, which are used to synthesize, along with the "flying" capacitor C_{fly}, three voltage levels at the switch node: $0, \frac{V_{in}}{2}, or V_{in}$. The converter has four independently control signals $\Phi_1 - \Phi_4$, which, if switched at the same frequency as the buck converter but with a 90° phase shift between them, multiplies the frequency seen by the output and passive components by four times.

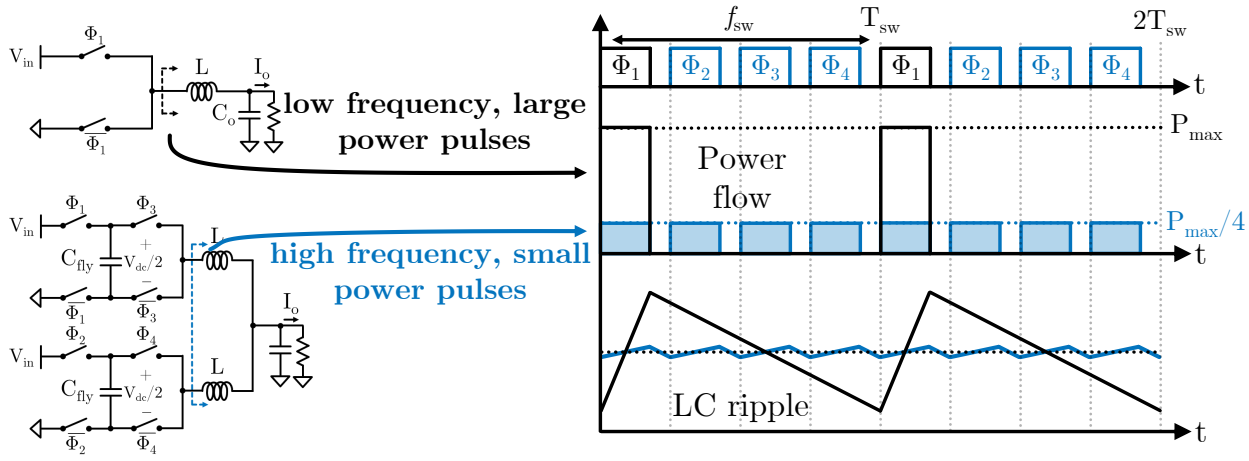


Figure 1.4: Principles of the effective multiplication of the power flow frequency and energy storage ripple achieved by using multiple multiplex switches.

This reduces the energy storage ripple, allowing the use of smaller, faster inductors and capacitors. This is a fundamental improvement on the buck converter's achievable efficiency and response speed, one which is agnostic to the particular components being used. In simple terms, multiplex switching *smooths* power delivery, and is analogous to why a four-cylinder engine is preferred to a thumper: it allows smaller bursts of power to be delivered at more frequent intervals for smoother power transfer. Using mutiple interleaved switches instead of few large switches also has the benefit of leveraging low-voltage devices that can switch faster [7], and multilevel designs in particular can replace inductor volume with energy dense clamping capacitors, which scale well to high frequency and high density designs [25, 31].

While the benefits of multiplex switching and frequency multiplication are clear, such designs are predicated on the switches being balanced, as they should evenly share the voltage and current stress (or at least proportionally to their size). However, in a lossless converter (indeed, in a lossless circuit in general), the distribution of multiple parallel currents and series voltages is not strictly defined – one phase may carry more current than the other, or one switch may block a higher voltage than the other [32]. This is problematic because the multiplex switches should be designed with voltage blocking and current carrying capability assuming balanced stress; if the switches were still sized to block the maximum unbalanced stress, the semiconductor area would be multiplied by the number of multiplex switches and would outweigh any frequency multipli-

cation benefits.

Balancing multiphase currents and multilevel voltages are both challenging [33]. Multilevel balancing is particularly critical because even momentary over-voltage can permanently damage a switch. Unfortunately, the more efficient a converter is, the weaker the effect of natural balancing from losses [34–37], which can cause significant imbalances between the multilevel voltages in practical converters [38]. Many methods have been proposed to balance multilevel converters, such as active balancing [39, 40], resistive networks [41], balance boosters [42], and optimizing the switching order [43], but all have drawbacks that limit their scalability: for example, requiring many additional components, having slow response, scaling poorly to higher frequencies, increasing loss, or lacking stability guarantees. One of the major contributions of this thesis, as detailed in section 1.2, is the presentation of a new, formal theory and robust, scalable methods based on coupled magnetics for balancing large-scale multilevel converters.

1.1.2 Background on Coupled Magnetics

Inductors are a key component in power electronics for energy storage, signal filtering, and current regulation. A "coupled" inductor is formed by winding two or more windings on a single magnetic core, as shown in Fig. 1.5(a). This causes the flux generated by each winding to interact with the other windings and induce EMF, thus coupling their currents and voltages. Coupled inductors are similar in function and construction to transformers; the main difference is that coupled inductors are designed and intended for energy storage, as opposed to purely energy transfer from one coil to another.

Coupled inductors, like transformers, can be modeled as magnetic circuits. As shown in Fig. 1.5(b), the coils can represented as flux (voltage) sources and the magnetic core represented by reluctances (resistances) that depend on the geometry and magnetic permeability. Coupled inductors are extremely important in multiphase converter design since they can reduce total inductor volume [31], reduce dynamic response time [5, 27], and reduce current ripple [26]. All of these benefits come from the coupling effect that allows each interleaved coil to affect the current in the others; the current ripple is reduced because the ripple frequency is multiplied by the num-

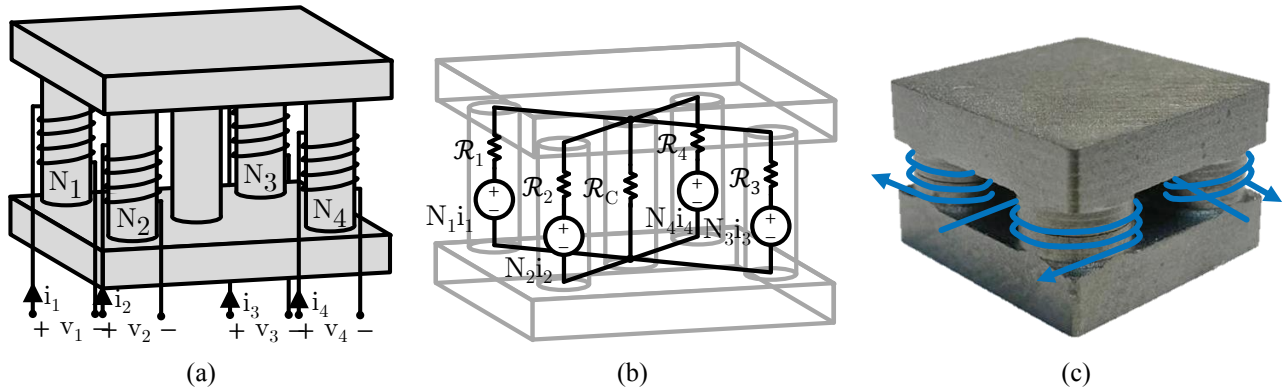


Figure 1.5: (a) Wireframe diagram of a basic four-phase coupled inductor structure, (b) associated magnetic circuit model, and (c) real magnetic core with windings (implemented with PCB traces in this work) illustrated.

ber of coils interleaved on the coupled inductor. Fig. 1.6 shows the four experimentally measured coil currents of a four-phase coupled inductor buck converter. The shape of the current ripples are characteristic of a coupled inductor converter; each coil is driven at 1 MHz, but because the excitation of each coil affects the other three, the effective current ripple frequency is multiplied by four to 4 MHz. This reduces the amplitude of the ripple, which reduces ac magnetic losses, or can be leveraged to reduce the size and response time of the magnetics.

Before this work, the intrinsic balancing benefits of combining coupled magnetics with multiplex switching were not known. This thesis develops a rigorous theoretical framework based on the reluctance model of coupled inductors to show how coupled magnetics passively balance multilevel voltages, then applies this principle to enable an order-of-magnitude increase in achievable multiplex switching. Prior works have also recognized how increasing the number of multilevel voltages in hybrid-switched-capacitor converters leads to complex and unpredictable converter dynamics [34, 43–46]. Converters with coupled inductors increase complexity even further by cross-coupling the passive components of multiple phases; this work addresses these challenges by developing simple new dynamic models for the internal dynamics of generalized converters with coupled passives and many multiplex switches.

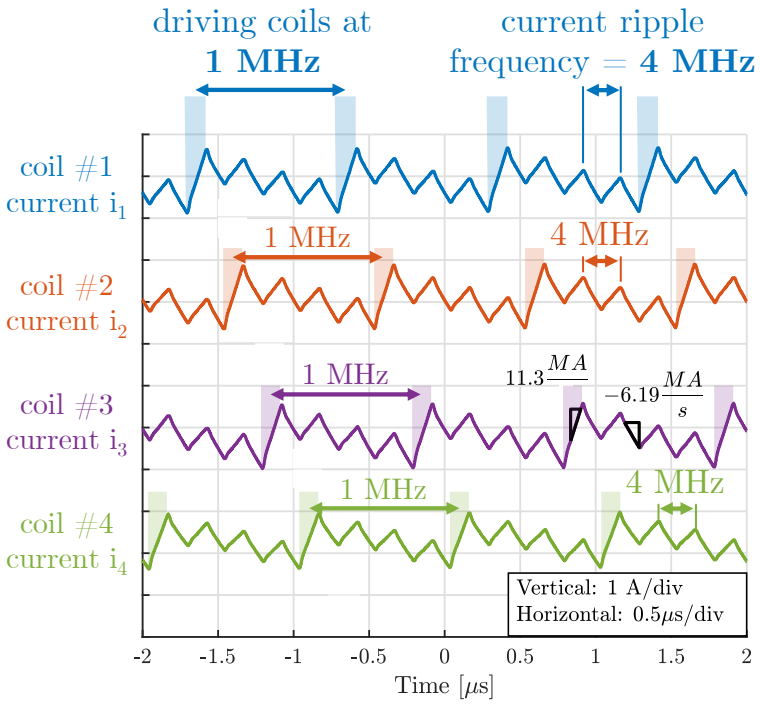


Figure 1.6: Example phase current ripples measured in a four-phase coupled inductor buck converter. The experimental details are contained in [5]

1.2 Dissertation Organization and Contributions

This work lays the foundation for a family of scalable power architectures leveraging multiplex switching and coupled magnetics. This work advances existing research in the field by developing a formal analysis framework for scalable power architectures, then using it to develop and explain a novel passive balancing technique for multiplex switching converters using coupled inductors, which addresses many of the drawbacks of existing methods. These theoretical frameworks and proposed techniques are demonstrated with state-of-the-art prototypes achieving an order-of-magnitude increase in converter performance and complexity. By studying power electronics on the architectural level, this work is broadly applicable to many scalable power converter topologies and many high-performance applications, with impacts that are agnostic to the particular components, power levels, or operating conditions.

This thesis is split into four chapters. Chapters 2 and 3 deal with theory that is broadly applicable to scalable power architectures regardless of components, application, and circuits. Chapter 4

and 5 deal with state-of-the-art demonstrations of the theory.

Specifically, chapter 2 intuitively, mathematically, and experimentally shows, for the first time, **how coupled magnetics can be used for balancing the voltage stress of scalable converters with many multiplex switches**, via:

- a framework for analyzing multilevel converter balancing based on feedback that is broadly applicable to analyzing passively balanced converters
- a rigorous proof showing how coupled inductors balance multiplex switches by providing a feedback path that cancels out external disturbances. By reducing the balancing question to a determinant problem, coupled inductors are proven to balance converters of arbitrary size, regardless of operating load, frequency, components, and with precisely defined singularities for certain duty ratios, coupling levels, and phase counts.
- an experimental demonstration of coupled inductors passively balancing multiphase, multilevel converters for the first time, verifying the mathematical results with a variety of converter sizes, components, and operating conditions.
- a set of simple design guidelines for coupled inductor FCML converters easily applicable to practical designs.

Chapter 3 **demystifies the multi-resonant dynamics of scalable power architectures with many multiplex switches and coupled passives**, via:

- a model for the internal dynamics of a generalized multiphase and multilevel converter with coupled passives. The internal dynamics are described, via analytical and computational modeling, as dependent on two parts: (i) the initial condition of the circuit, which determines which of the multi-resonant modes of a large-scale (degree > 2) converter are excited, and (ii) the eigenstructure, which describes the quantitative effect of key parameters such as the switching frequency, quality factor, and magnitude of loss.

- development of two complementary mathematical frameworks for understanding the internal converter dynamics, one based on power dissipation yielding analytical results for simple converters, and one state-space model for arbitrary converters. The power dissipation model, in particular, reveals the importance of for the power dissipation "context" and how it affects the internal dynamics of many existing converters
- an experimental verification of both the analytical and computational results, with a correct prediction, for the first time, of the multi-resonant behavior.

Chapter 4 applies and experimentally proves the theory of the previous two chapters and **demonstrates an order-of-magnitude scale-up of achievable switching complexity and frequency multiplication from current state-of-the-art research**, yielding:

- a four-phase, 17-level FCML converter that multiplies the effective switching frequency by $64\times$, a state-of-the-art achievement. This level of frequency multiplication results in extremely small passive requirements and dramatically accelerated output response time.
- the balancing of 60 flying capacitors with one four-phase coupled inductors without active control, a leading result that enables the order-of-magnitude scale-up of switch count.
- above-switching-frequency output modulation. Having achieved a new level of balanced frequency multiplication, the converter output can be modulated at a frequency higher than the switching frequency. In this region of output signal modulation, the amplitude as well as the frequency (in the sense of Nyquist sampling) must be considered; an information theoretical description of the amplitude-frequency limits of above-switching-frequency modulation of generalized multiplex switching converters is provided.

Chapter 5 again applies the theories of chapters 2 and 3 and the circuits in chapter 4 to the **signal-over-power application space**, linking the impacts of this thesis to communication systems by **designing a state-of-the-art, high-power, high-speed visible light communication transmitter for Li-Fi (light fidelity) applications**, specifically achieving:

- 1000 W of wide-angle LED illumination converted with 95.8% efficiency (including all gate drive/auxillary losses) and simultaneous communication at 6.4 Mbps and 8.03% EVM at a distance of 20 meters.
- a high performance four-phase, seven-level FCML converter leveraging high frequency, low voltage devices balanced by four-phase coupled inductors. The design achieves high density (17 mm^2 total area including gate drive) and develops a novel floating gate drive circuit that maximizes efficiency and eliminates the external bootstrap supply such that only one input supply.
- cross-disciplinary impact on communications systems by showing how balanced, scalable power architectures can provide high-power, high-efficiency power conversion and high-frequency, high-throughput communications simultaneously for various “talkative power” applications such as Li-Fi, power line communications (PLC), and impedance measurement.

Finally, chapter 6 concludes this thesis and presents potential future work.

2

Balancing Scalable Power Architectures using Coupled Magnetics

The contents of this chapter were previously published under D. H. Zhou, J. Čeliković, D. Maksimović, and M. Chen, IEEE Transactions on Power Electronics, 2024.

Abstract

This chapter investigates the modeling, analysis, and design methods for passively balancing flying capacitor multilevel (FCML) converters using coupled inductors. Coupled inductors synergize with FCML converters by reducing inductor current ripple, reducing switch stress, and, as proven in this chapter, by providing flying capacitor voltage balancing. This enables FCML topologies to be scaled well to larger systems. This chapter proves that coupled inductors can solve the unbalancing problem in many FCML converters. Moreover, tools are developed to thoroughly explain and quantify coupled inductor balancing, allowing general design guidelines to be offered for robust coupled inductor FCML converters. Finally, this chapter derives the limitations of coupled inductor balancing with respect to the number of phases, levels, and the required coupling ratio. The key principles of coupled inductor FCML balancing in steady-state are demonstrated with a systematic theoretical framework and extensive experimental and simulation results.

2.1 Chapter Introduction

Multilevel converters are an important enabling technology for power converter applications requiring low current ripple and fast transient response, such as CPU voltage regulators [24, 47], envelope trackers, and power amplifiers [13, 48]. By using three or more switching voltage levels, multilevel converters can reduce the voltage and current stress on components and multiply the effective switching frequency. One method of generating more than the two switching voltage levels from a single input voltage is to use capacitors with dc voltages connected in series with the input supply. This is the working principle of flying capacitor multilevel (FCML) converters [30], which have proved especially effective in high bandwidth and high power converter designs [12, 34–37, 42, 49–51].

Multilevel converters help to address one of the fundamental challenges of high bandwidth power converter designs: the trade-off between current ripple and bandwidth presented by the in-

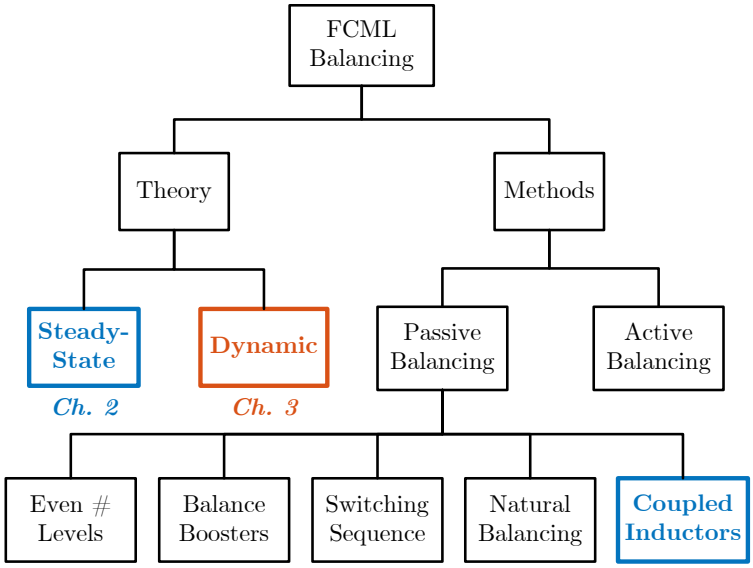


Figure 2.1: Chart of selected research areas in FCML converter balancing. Coupled inductors represent a new branch of techniques for passively balancing FCML converters which can be used together with other techniques. Some of the highlighted balancing methods are compared in Section 2.7.

ductive elements [47, 48, 52]. It is desirable to have a larger inductance to maintain low inductor current ripple, but it is also desirable to have a smaller inductance to respond to sudden load, input line, or output reference transients [49, 50, 53]. For a buck converter, the inductor selection must trade-off these two competing criteria. By switching between voltage levels that are closer together at a higher effective switching frequency, multilevel converters enable the use of smaller inductors without increasing the current ripple, thus circumventing the typical inductor trade-off.

FCML converters also synergize well with multiphase coupled inductors. Interleaving multiple converter phases with coupled inductors can reduce the inductor size [54], output current ripple [55], and transient inductance [5, 27]. Since coupled inductors reduce not only the overall current ripple but also that of the individual phases [26, 56], they can also reduce the core loss and saturation flux requirements. Finally, as proven in this chapter, interleaving multiple FCML converters with coupled inductors passively balances the flying capacitors, overcoming the key limitation of FCML converters.

2.1.1 Background on Multilevel Converter Balancing

Despite their numerous advantages in theory, FCML converters only function well if the flying capacitors stay at their ideally balanced voltage levels. If the flying capacitors are not balanced, the switching voltage levels will become corrupted and cause increased voltage stresses, current ripple, and harmonic distortion at the output [35, 37, 57]. Considerable attention has been given to understanding the theory of flying capacitor balancing and developing improved methods for balancing a single-phase, standalone FCML converter.

It has been shown that practical FCML converters exhibit natural balancing [34, 43, 45]. In this chapter, we define natural balancing as the process in which the power losses in the converter gradually balance the flying capacitors to their ideal values. Ideal odd-level FCML converters have been shown to exhibit steady-state indeterminacy, which leads to an increased sensitivity of flying capacitor voltages to parasitic losses and timing imperfections [32]. Therefore, natural balancing can be less reliable, especially when losses are low. Moreover, the variable and nonlinear nature of natural balancing makes it difficult to predict the steady-state flying capacitor voltage imbalance and to size the component ratings [46, 58, 59].

Many other methods of balancing flying capacitors have been developed, some of which are shown in Fig. 2.1. Perhaps the most prominent is active balancing, where the flying capacitor voltages are sensed or estimated and then balanced through an active intervention such as adjusting the phase shift or duty cycles of the switches [39, 40, 60, 61]. This is a flexible and robust technique that is applicable in many FCML converters. However, since active balancing requires additional sensing circuitry and more complex control, it becomes challenging to implement as the number of levels, the switching frequency, or the control bandwidth increase [58, 61]. Other approaches such as balance boosters [42], optimizing the switching sequence [43, 62, 63], or simply choosing an even number of levels [59] seek to improve the passive balancing of FCML converters. Here, we define passive balancing as any balancing mechanism that does not use active control to sense and adjust the flying capacitor voltages. Therefore, natural balancing is a type of passive balancing.

In addition to the practical methods used to balance FCML converters, the underlying theory of how flying capacitors are balanced can be divided into two broad categories: i) dynamic, which describes how FCML converters dynamically balance (or fail to do so) from an initial imbalance [35, 37, 43], and ii) steady-state, which describes the flying capacitor imbalance that persists at steady-state due to external unbalancing mechanisms. In particular, while much early FCML balancing research focuses on dynamic behavior, [38] studies the existence of steady-state imbalances and examples of practical non-idealities that can cause them.

2.1.2 Using Coupled Inductors to Balance Scalable Multiphase, Multilevel Converters

One recent advance is the use of coupled inductors to balance multiphase FCML converters in dynamic [64] and steady-state conditions [65], and with multiple phases and levels [66]. By coupling the inductor currents of multiple interleaved FCML converters, the flying capacitors of one phase can compensate the imbalances of another and passively balance the system. This offers several advantages over other means of balancing: i) The FCML converter system naturally inherits the benefits of coupled inductors in current ripple reduction and faster transient response; ii) Coupled inductors provide lossless flying capacitor voltage balancing without any additional components or changes to the switching scheme that is much stronger than natural balancing in most practical converters; iii) Coupled inductor balancing scales well to higher power levels, large numbers of levels, and higher switching frequencies since there is no need to sense or actively adjust the flying capacitor voltages. However, no systematic analysis has been presented to quantitatively explain the balancing mechanisms of coupled inductors and to explore their applicability and limitations.

2.1.3 Contributions of this Work

This chapter systematically investigates the mechanisms, applicability, and limitations of coupled inductor balancing of FCML converters. The main contributions are:

- We develop, for the first time, a systematic modeling framework for quantitatively describing the balancing behavior of coupled inductor FCML converters. The models and meth-

ods scale well to an arbitrary number of levels, number of phases, and switching pattern.

- We compare coupled inductor balancing to other common techniques such as active balancing and demonstrate its advantages in cost, strength, and flexibility.
- We analyze the limitations of scaling the technique to an arbitrary number of levels and phases, and explore the scenarios when the balancing mechanisms may fail. Balancing with partially coupled inductors is discussed, including desirable regions of coupling to maximize robustness.
- While this chapter deals mainly with coupled inductor balancing, the modeling methods and framework are broadly applicable to other FCML converter balancing mechanisms.

The rest of the chapter is organized as follows: Section 2.2 reviews the background of FCML converters and coupled inductors. Section 2.3 explains the fundamental balancing mechanism of coupled inductors. Section 2.4 derives a systematic mathematical framework for studying coupled inductor balancing and to determine which converters coupled inductors can balance. Section 2.5 finds the limitations of coupled inductor balancing with regards to the number of phases, levels, and coupling ratio. Section 2.6 verifies the theoretical results using a four-phase, three-level FCML converter and a two-phase, five-level FCML converter. Section 2.7 compares coupled inductor balancing to other common techniques including active balancing, natural balancing, and even-level selection. General design guidelines for coupled inductor FCML converters to minimize capacitor voltage imbalances are reviewed. Finally, we summarize our main findings in Section 2.8.

2.2 Multiphase FCML Converters with Coupled Inductors

Figure 2.2 shows a two-phase, three-level FCML converter with coupled inductors used as the canonical cell for presenting the analytical framework. The two phases each have two pairs of switches operated as complementary pairs to prevent shorting. The switches signals are labelled as Φ_{xy}, where x is the phase number and y orders the switches in one phase with $y = 1$ being

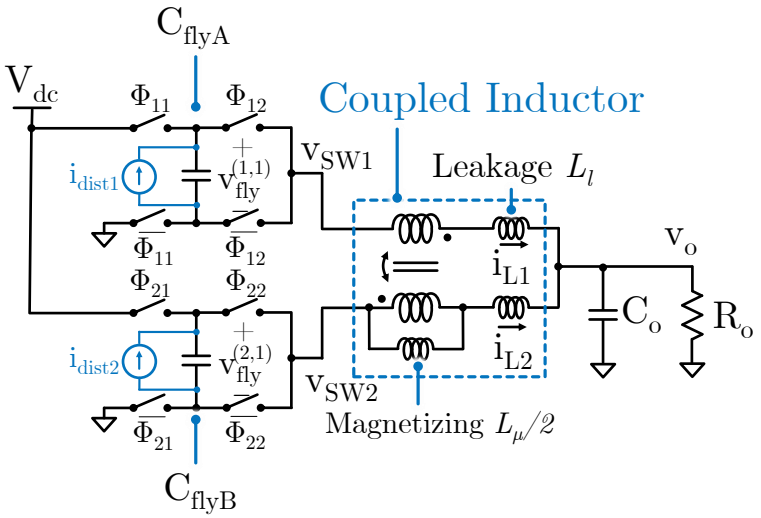


Figure 2.2: Schematic of a two-phase, three-level FCML converter with coupled inductors parameterized by the leakage (L_l) and magnetizing (L_μ) inductance. The current sources i_{dist1} and i_{dist2} model mechanisms unbalancing the flying capacitors, such as timing or duty cycle mismatches.

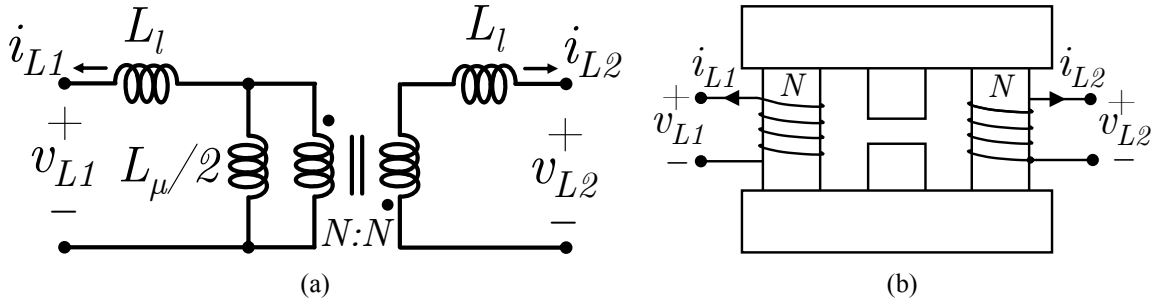


Figure 2.3: (a) Schematic and (b) diagram of a two-phase coupled inductor parameterized using leakage and magnetizing inductance.

closest to the input side. Each phase has a flying capacitor, labeled C_{fly1} and C_{fly2}, which ideally have voltages equal to half the input voltage V_{dc} such that the switch node voltages can be 0, $\frac{V_{\text{dc}}}{2}$, or V_{dc} depending on the switch connections. The phases are coupled by a two-phase coupled inductor, which is also illustrated in Fig. 2.3. The coupled inductor is parameterized using a transformer model and its leakage and magnetizing inductance, L_l and L_μ. Additional background on multiphase coupled inductors and models used in this chapter can be found in Appendix I.

Fig. 2.4 shows the switching waveforms of the converter, with the switch states and capacitor charge/discharge states detailed in Table 2.1. Both of the individual FCML converter phases are switched using phase-shifted pulse width modulation (PS-PWM), which means the switch pairs in one phase are operated with a duty cycle of d and phase shifted by 180° to distribute the

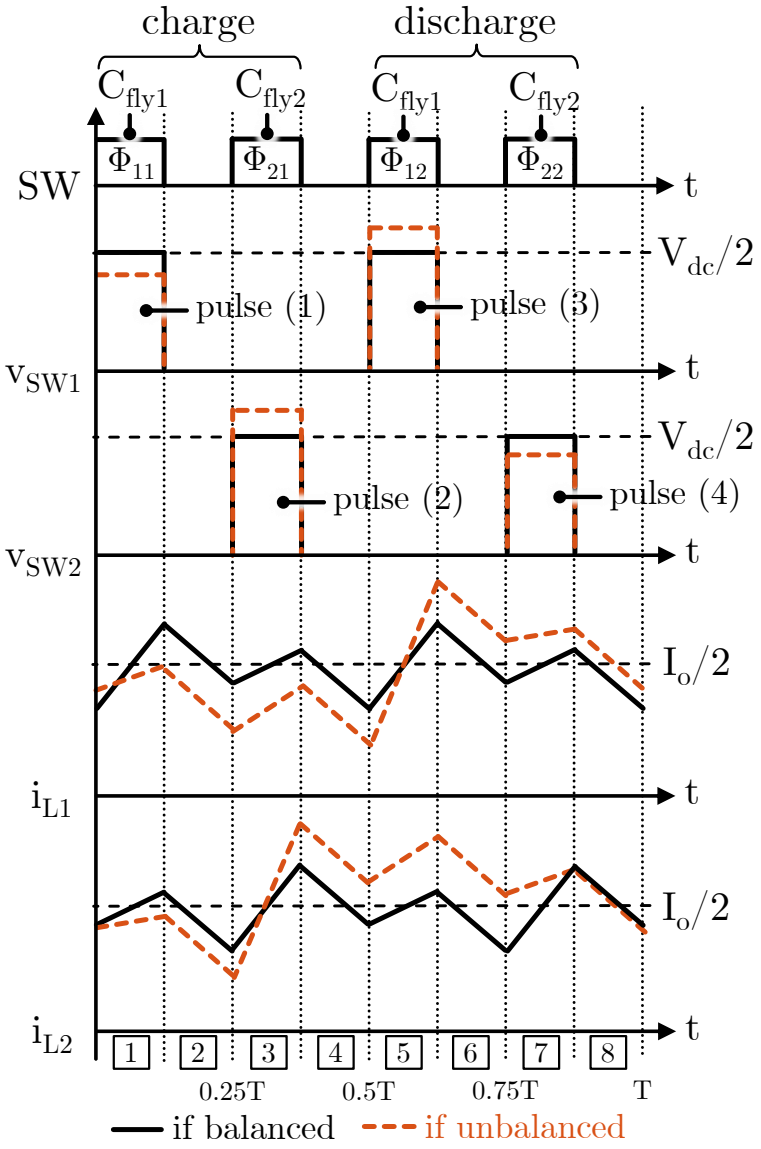


Figure 2.4: Switching waveforms of the two-phase, three-level FCML converter in Fig. 2.2 with PS-PWM and $d = 0.125$. If the flying capacitors are imbalanced (illustrated with a positive imbalance on phase #1 and a negative imbalance on #2), the current ripple is increased.

Table 2.1: Switch and flying capacitor states for two-phase, three-level FCML converter with $d = 0.125$

Sub-period	1	2	3	4	5	6	7	8
Start time t	0	$\frac{T}{8}$	$\frac{T}{4}$	$\frac{3T}{8}$	$\frac{T}{2}$	$\frac{5T}{8}$	$\frac{3T}{4}$	$\frac{7T}{8}$
Φ_{11}	1	0	0	0	0	0	0	0
Φ_{21}	0	0	0	0	1	0	0	0
Φ_{21}	0	0	1	0	0	0	0	0
Φ_{22}	0	0	0	0	0	0	1	0
C_{flyA}	chg	-	-	-	dischg	-	-	-
C_{flyB}	-	-	chg	-	-	-	dischg	-

switching actions evenly in the switching period T. The two phases are then themselves interleaved with a phase shift of 90°. The result of this dual interleaving is four evenly interleaved switch pulses, labelled pulse (1) through pulse (4) in Fig. 2.4. For higher numbers of phases or levels in the FCML converter, the switches are similarly interleaved such that the switching events are always uniformly distributed in a cycle.

During pulse (1), phase #1 connects V_{dc} to v_{SW1} through C_{fly1} and charges the flying capacitor. During pulse (2), phase #2 connects V_{dc} to v_{SW2} through C_{fly2} and charges the flying capacitor. Pulses (3) and (4) connect the switch nodes to ground through the flying capacitors in the opposite direction, which discharges them. Since the ideal voltage of the flying capacitors is $\frac{V_{\text{dc}}}{2}$, each of the four switch node voltage pulses are ideally at $\frac{V_{\text{dc}}}{2}$.

With uncoupled inductors, the current in each phase i_{L1} and i_{L2} will ramp based only on the voltage applied to the same coil. Only natural balancing is in effect. When the inductors are coupled, the currents also ramp depending on the voltage of the other phase. This happens because of the shared magnetic flux paths as shown in Fig. 2.3(b). To quantify the amount of coupling between the phases, we define the inductive relationships between the phases as

$$\begin{bmatrix} \frac{\mathrm{d}i_{L1}}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{L2}}{\mathrm{d}t} \end{bmatrix} = \underbrace{\begin{bmatrix} 1/L_{\text{same}} & 1/L_{\text{cross}} \\ 1/L_{\text{cross}} & 1/L_{\text{same}} \end{bmatrix}}_{\mathcal{L}^{-1}} \begin{bmatrix} v_{L1} \\ v_{L2} \end{bmatrix}, \tag{2.1}$$

where the inductor voltages and currents are labelled in Fig. 2.3(a). Matrix $\mathcal{L}^{-1}$ is the inverse

of the inductance matrix $\mathcal{L}$ in $\mathbf{v_L} = \mathcal{L}\frac{\mathbf{di_L}}{\mathbf{dt}}$ describing the induced voltages in each coil due to changing coil currents. $\mathcal{L}$ is traditionally parameterized by the self and mutual inductances [26]. The formulation in eq. (2.1) is inverted, with changing currents expressed as a function of applied voltages: $\frac{\mathbf{di_L}}{\mathbf{dt}} = \mathcal{L}^{-1}\mathbf{v_L}$. To avoid confusion with the self and mutual inductances, we define the *same inductance* (L_{same}) describing the resulting current ramp if a voltage is applied to the same winding, and the *cross inductance* (L_{cross}) describing the current induced in one phase if the other has a voltage applied to it. According to [26], L_{cross} and L_{same} are functions of the mutual and leakage inductance L_μ and L_l:

$$L_{\text{cross}} = \left(\frac{M-1}{\mu} + M\right) L_l, \tag{2.2}$$

$$L_{\text{same}} = \frac{\mu}{M-1+\mu}\left(\frac{M-1}{\mu} + M\right) L_l, \tag{2.3}$$

where M is the number of phases and $\mu = \frac{L_\mu}{L_l}$ is the coupling ratio. L_{cross} is always greater than or equal to L_{same}. When $\mu \to \infty$, the inductors becoming fully coupled and $L_{\text{cross}} = L_{\text{same}} = ML_l$, indicating that applied phase voltages have equal influence on all phase current.

Fig. 2.4 shows the inductor current waveforms in the two-phase example that are typical of a coupled inductor system. For example, the current in phase 2 increases during sub-period #1 despite the fact that the voltage on its coil is $-V_o$ during this time. This is because the first coil has a positive voltage and is coupled to it. The current in phase 2 will not necessarily increase during sub-period #1 depending on the coupling ratio [26], but its slope will always be greater than if there was no coupling.

Because a voltage applied on either coil ramps the current in both, the current ripple frequency is doubled from usual and the ripple is reduced. Increasing the coupling ratio increases the effect that the voltage on one coil has on the current in the other. A fully coupled inductor, where the flux in each phase is identical, would have $L_{\text{cross}} = L_{\text{same}}$ and the same current (both dc current and ac ripple) in both phases. With tight coupling, it is important to switch all phases with

proper phase shifting, as the core will present a low inductance if only one phase is switched and be prone to saturation.

If the flying capacitor voltages are not equal to $V_{\text{dc}}/2$, they are unbalanced. Fig. 2.4 illustrates this for the case where flying capacitor #1 has a positive imbalance and flying capacitor #2 has a negative imbalance. In this case, the switch node pulses have voltages above and below the ideal level, which increases the current ripple. Moreover, the voltage stress on the switches is increased. This is why it is important to ensure the flying capacitor voltages remain balanced.

Later sections of this chapter deal with FCML converters with more phases and levels. We define the number of phases as M and the number of flying capacitors in each phase as K. Each phase is therefore a $(K+2)$-level FCML converter since the number of possible switching levels is always two more than the number of flying capacitors. We denote the flying capacitor voltages as $v_{\text{fly}}^{(\text{phase \#m, cap \#k})}$, or for brevity, $v_{\text{fly}}^{(\text{m,k})}$, where $m = 1, \ldots, M$ and $k = 1, \ldots, K$ are the indices identifying the phase and capacitor. The capacitor closest to the input source has the index $k = 1$. The ideally balanced flying capacitor voltages in this case are

$$v_{\text{fly, balanced}}^{(\text{\#m, \#k})} = V_{\text{dc}} \frac{K+1-k}{K+1}, \tag{2.4}$$

which are the voltages that result in equal voltage stresses on all switches and switching levels that are evenly spaced between 0 and V_{dc}.

2.3 Fundamental Principles of Coupled Inductor FCML Converter Balancing

In this section, we present a feedback framework to explain the mechanisms of coupled inductor voltage balancing for FCML converters. In the context of this chapter, we define voltage balancing as the flying capacitor voltages reaching steady-state values, and we are interested in understanding the mismatches between these steady-states and the nominal capacitor voltages. We start by formally reviewing small-signal modelling of FCML converter balancing. Then, we show how the losses in a FCML converter will naturally force the system into a steady-state, regardless of if the inductors are coupled or uncoupled, then compare the resulting steady-state values in the

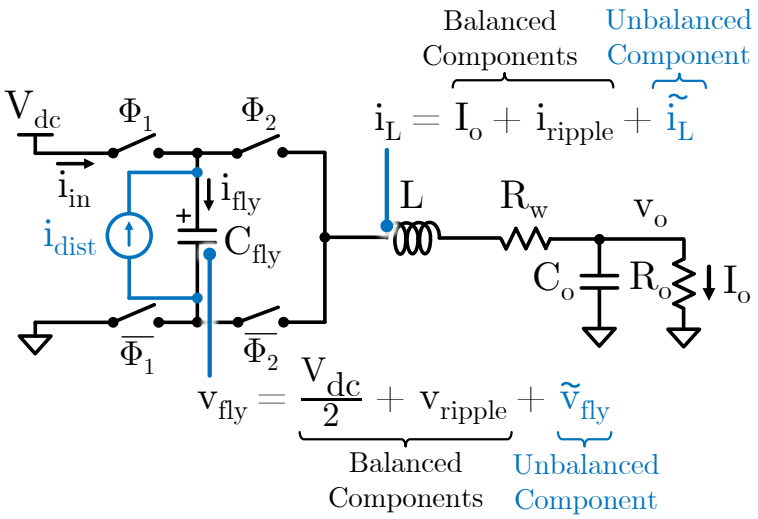


Figure 2.5: Schematic of a three-level FCML converter with separation of balanced and unbalanced components of state variables.

uncoupled and coupled cases.

2.3.1 Small-Signal Modeling of FCML Converter Balancing

In this section, we formalize the small-signal modelling principles used to develop the feedback models in the proceeding sections. First, we examine the schematic of the three-level converter in Fig. 2.5. The state variables are the inductor current i_L and the flying capacitor voltage v_{fly}. These state variables can be further divided by superposition into balanced and unbalanced components. This division simplifies the analysis since only the unbalanced components, the flying capacitor voltage imbalance $\tilde{v}_{\text{fly}}$ and the inductor current imbalance $\tilde{i}_L$, are relevant to balancing analysis. The large-signal load current I_o, the ideally balanced voltage flying capacitor, $V_{\text{dc}}/2$, and the switching ripple (which we assume to be negligible) are components of normal operation that can be ignored. Therefore, each flying capacitor voltage is written as

$$v_{\text{fly}}^{(m,k)} = v_{\text{fly, balanced}}^{(m,k)} + \tilde{v}_{\text{fly}}^{(m,k)}, \tag{2.5}$$

where the balanced level is defined in eq. (2.4). Fig. 2.6 shows the switching waveforms of the three-level converter. We wish to relate the imbalance voltage, power loss, and current in the flying capacitor. In our analysis, we assume the power loss comes from the resistance in series with

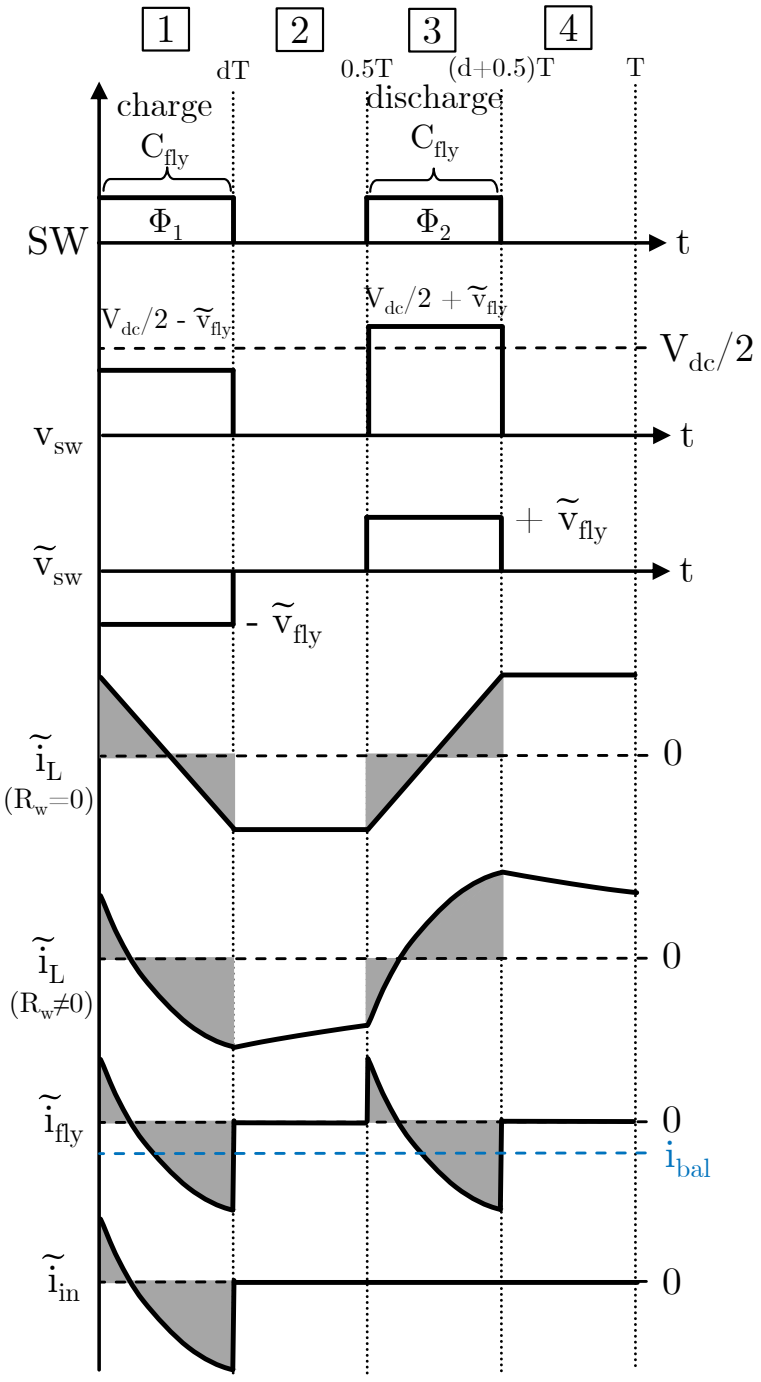


Figure 2.6: Switching waveforms of a single-phase three-level FCML converter. The unbalanced component of the switch node voltage causes a perturbation of the inductor current, $\tilde{i}_L$. If the resistance R_w is zero, the inductor current perturbation ramps linearly and causes no charge transfer in the flying capacitor. If the resistance is nonzero, the inductor current ramps exponentially and there is a net charge transfer, thus causing lossy natural balancing.

the inductor R_w. First, we analyze how an imbalance in the flying capacitor affects power transfer in the converter. There are four sources and sinks of power in the converter in Fig. 2.5: i) power dissipated in the resistance, ii) power input from the source V_{dc}, iii) power output to the load, and iv) power that charges the flying capacitor. First, we compute the loss that an unbalanced flying capacitor causes in the resistor. Fig. 2.6 shows the switching waveforms of the three-level converter. By superposition, the imbalanced component of the flying capacitor voltage, $\tilde{v}_{\text{fly}}$, is applied to the switch node twice in alternating directions every period. This induces an imbalanced component of the inductor current ripple $\tilde{i}_L$. Assuming the flying capacitor is large enough such that the flying capacitor voltage does not change appreciably during a switching period, induced current is symmetric across $t = 0.5T$ and has zero mean. This assumption is valid because the flying capacitors must be sized large enough to minimize the ripple at maximum load and protect the switches. Averaging over a switching period, the unbalanced inductor current causes an average power loss in the resistance R_w

$$\begin{aligned}\langle P_{R_w} \rangle &= \left\langle R_w i_L^2 \right\rangle = \left\langle R_w (I_o + \tilde{i}_L)^2 \right\rangle \\ &= R_w I_o^2 + R_w \left\langle \tilde{i}_L^{\,2} \right\rangle + R_w I_o \cancelto{0}{\langle \tilde{i}_L \rangle} \\ &= R_w I_o^2 + R_w \left\langle \tilde{i}_L^{\,2} \right\rangle . \end{aligned} \tag{2.6}$$

Here, $\langle x(t) \rangle = \frac{1}{T} \int_0^T x(t)\, \mathrm{d}t$ represents the average over a switching period. Because the FCML converter switches the flying capacitor in alternating directions symmetrically every period, the inductor imbalance current is symmetric about zero and has zero mean, meaning the loss components from the large- and small- signal current are independent. Next, the output power is

$$P_o = I_o (d V_{\text{dc}} - R_w I_o), \tag{2.7}$$

assuming the output capacitor is very large such that the output voltage is constant. The flying capacitor current is equal to the inductor current with alternating directions as shown in Fig. 2.6. The power transferred to the flying capacitor is

$$\langle P_{\text{fly}} \rangle = \left(\frac{V_{\text{dc}}}{2} + \tilde{v}_{\text{fly}} \right) \langle \tilde{i}_{\text{fly}} \rangle . \tag{2.8}$$

Finally, power comes from the input source. The input current sees the same imbalance current as the flying capacitor during $0 < t \leq dT$. The flying capacitor current during $0.5T < t \leq (d+0.5)T$ is identical to $0 < t \leq dT$, but the input source is not connected during this time. Therefore, the average current from the source is equal to the average capacitor current divided by two. The average power from the source is

$$\langle P_{\text{in}} \rangle = dV_{\text{dc}} I_o + V_{\text{dc}} \frac{\langle \tilde{i}_{\text{fly}} \rangle}{2}. \tag{2.9}$$

By conservation of energy, the average power of all sources and sinks sums to zero:

$$\begin{aligned}
&\langle P_{\text{in}} \rangle - P_o - \langle P_{\text{fly}} \rangle - \langle P_{R_w} \rangle = 0 \\
&\underbrace{dV_{\text{dc}} I_o + V_{\text{dc}} \langle \tilde{i}_{\text{fly}} \rangle / 2}_{\langle P_{\text{in}} \rangle} - \underbrace{(I_o dV_{\text{dc}} - R_w I_o^2)}_{P_o} \\
&\quad - \underbrace{\left(\frac{V_{\text{dc}}}{2} + \tilde{v}_{\text{fly}} \right) \langle \tilde{i}_{\text{fly}} \rangle}_{\langle P_{\text{fly}} \rangle} - \underbrace{\left(R_w I_o^2 + R_w \left\langle \tilde{i}_L^{\,2} \right\rangle \right)}_{\langle P_{R_w} \rangle} = 0 \\
&\qquad \rightarrow -\tilde{v}_{\text{fly}} \langle \tilde{i}_{\text{fly}} \rangle - R_w \left\langle \tilde{i}_L^{\,2} \right\rangle = 0 \\
&\qquad \rightarrow \tilde{i}_{\text{bal}} := \langle \tilde{i}_{\text{fly}} \rangle = -\frac{R_w \left\langle \tilde{i}_L^{\,2} \right\rangle}{\tilde{v}_{\text{fly}}}.
\end{aligned} \tag{2.10}$$

The average current into the flying capacitor, which we define here as the balancing current $\tilde{i}_{\text{bal}}$, is dependent only on the "small-signal" loss in the resistor $R_w \left\langle \tilde{i}_L^{\,2} \right\rangle$ and the flying capacitor voltage. It is not dependent on the large-signal input voltage or load current. This happens because for every unit of charge taken from the flying capacitor, a proportional unit is taken from the input source. In other words, the small-signal power loss affects the small-signal flying capacitor voltage, while the large-signal flying capacitor voltage is taken care of by the input source. The balancing effect always reduces the flying capacitor imbalance. Since the power loss is always

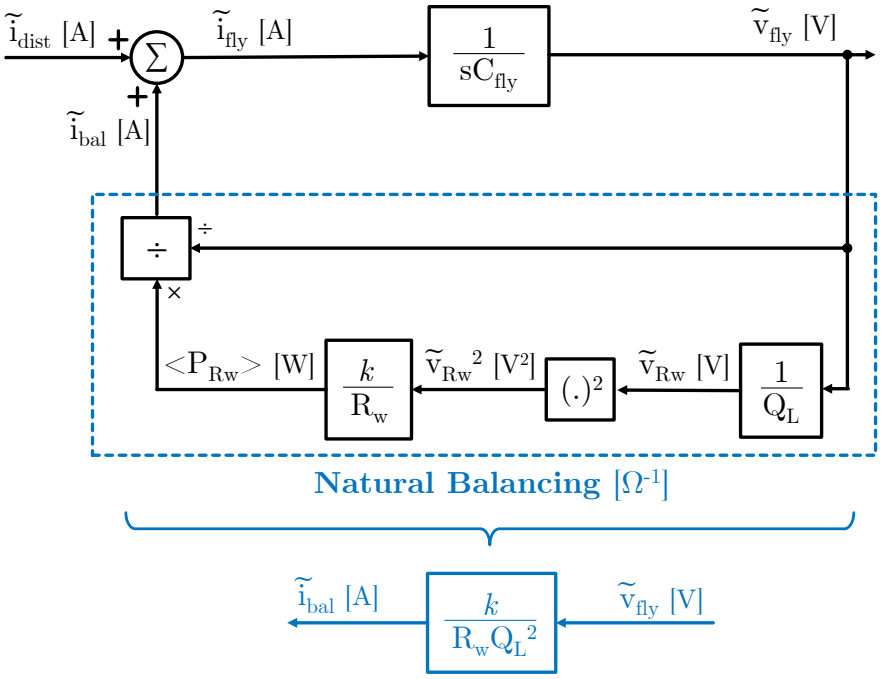


Figure 2.7: Feedback diagram of natural balancing in standard FCML converter, where power losses provide the balancing action.

positive, if the flying capacitor imbalance voltage $\tilde{v}_{\text{fly}}$ is positive, $\tilde{i}_{\text{bal}}$ is negative and the flying capacitor is discharged by the power loss, and vice versa if the imbalance is negative.

2.3.2 Feedback Model of Natural Balancing

We develop a model for natural balancing using the single-phase FCML converter shown in Fig. 2.5 to compare it to the canonical coupled two-phase case. FCML converters exhibit natural balancing, where flying capacitor imbalance voltages cause increased losses that dissipate the imbalance gradually [34, 35, 37, 57, 67]. For converters without balancing techniques like active balancing, natural balancing is the dominant mechanism that determines the flying capacitor voltages.

Assuming the inductor resistance R_w provides the loss source, the "small-signal" power loss $\langle \tilde{P}_{R_w} \rangle$, considering only the unbalanced state variables, is

$$\langle \tilde{P}_{R_w} \rangle = \frac{\gamma}{R_w Q_L^2} \tilde{v}_{\text{fly}}^2, \tag{2.11}$$

where $\gamma = \frac{d^2(3-4d)\pi^2}{3}$ is a scaling factor depending on the duty cycle and $Q_L = \frac{\omega_{\text{sw}} L}{R_w}$ is the quality

factor of the inductor at the switching frequency. The details of this calculation are contained in Appendix II. The power loss is equal to the approximate imbalance voltage over the resistor $\frac{\tilde{v}_{\text{fly}}}{Q_L}$ squared, divided by the winding resistance R_w and scaled by γ. As proven in Section 2.3.1 (and verified in Appendix II), this power loss causes an effective balancing current

$$\tilde{i}_{\text{bal}} = \frac{\left\langle \tilde{P}_{R_w} \right\rangle}{\tilde{v}_{\text{fly}}} = \frac{\gamma}{R_w Q_L^2} \tilde{v}_{\text{fly}}. \tag{2.12}$$

Equation (2.12) relates the balancing current to the power loss, and by extension, the imbalance voltage. Using these equations, we construct the feedback model of natural balancing shown in Fig. 2.7. The flying capacitor is modelled as an integrator of current that produces an imbalance $\tilde{v}_{\text{fly}}$ which feeds back via natural balancing to counteract external disturbances modelled using $\tilde{i}_{\text{dist}}$. The flying capacitor imbalance voltage $\tilde{v}_{\text{fly}}$ induces an average power loss $\langle P_{R_w} \rangle$ depending on the quality factor of the inductor Q_L.

The feedback diagram emphasizes the fundamental problems with natural balancing: it relies on large converter losses to be effective. The steady-state gain from disturbance to imbalance, which we compute by setting $\tilde{i}_{\text{dist}} = -\tilde{i}_{\text{bal}}$, is

$$\left.\frac{\tilde{v}_{\text{fly}}}{\tilde{i}_{\text{dist}}}\right|_{\text{steady-state}} = \frac{Q_L^2 R_w}{\gamma}. \tag{2.13}$$

If the quality factor Q_L of the inductor is high, the gain from imbalance voltage to balancing current will be low, leading to weak balancing capability.

2.3.3 Feedback Model of Coupled Inductor Balancing

Coupled inductor balancing uses a fundamentally different mechanism to natural balancing. Fig. 2.8 illustrates the balancing mechanism in a feedback model for a two-phase FCML converter with coupled inductors. An imbalance voltage on either phase will induce a current in the other through the coupled inductors. We show that in periodic steady state, coupled inductors create a negative feedback loop through the cross inductance L_{cross} to greatly mitigate the voltage imbalance created by an external disturbance. This mechanism is significantly more effective

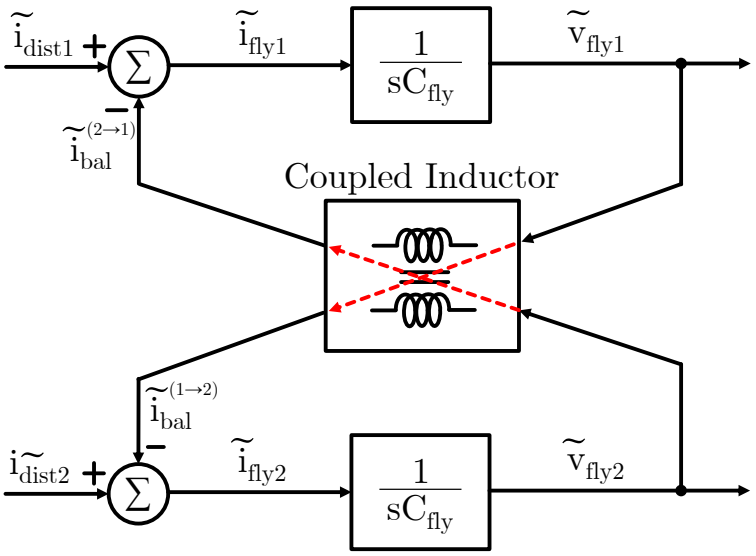


Figure 2.8: Feedback diagram of two-phase, three-level FCML converter balanced by coupled inductors.

than the lossy mechanism of natural balancing because its gain is much higher.

Fig. 2.9 details the coupled inductor feedback loop. Through the coupled currents, the imbalance voltage of phase #2 can compensate for the disturbance current in phase #1 and vice versa. Both phase imbalances induce currents in the other with slope $1/L_{cross}$ and scaled by a timing factor derived in Appendix II. In the $0 < d < \frac{1}{4}$ case, this timing factor has magnitude d^2T because the induced current ramps up for dT and then the balanced flying capacitor is connected for duration dT, so the average balancing current is scaled by $dT \times dT / T = d^2T$.

The closed-loop transfer functions from $\{\tilde{i}_{dist1}, \tilde{i}_{dist2}\}$ to $\{\tilde{v}_{fly1}, \tilde{v}_{fly2}\}$, which are computed by dividing the forward gain by the loop gain, are

$$\left.\begin{bmatrix}\tilde{v}_{fly1}\\ \tilde{v}_{fly2}\end{bmatrix}\right|_{coupled} = \begin{bmatrix}\frac{\frac{1}{sC_{fly}}}{1-(\frac{d^2T}{L_{cross}}\frac{1}{sC_{fly}})^2} & \frac{-\frac{d^2T}{L_{cross}}(\frac{1}{sC_{fly}})^2}{1-(\frac{d^2T}{L_{cross}}\frac{1}{sC_{fly}})^2}\\ \frac{\frac{d^2T}{L_{cross}}(\frac{1}{sC_{fly}})^2}{1-(\frac{d^2T}{L_{cross}}\frac{1}{sC_{fly}})^2} & \frac{\frac{1}{sC_{fly}}}{1-(\frac{d^2T}{L_{cross}}\frac{1}{sC_{fly}})^2}\end{bmatrix}\begin{bmatrix}\tilde{i}_{dist1}\\ \tilde{i}_{dist2}\end{bmatrix}. \tag{2.14}$$

The steady state dc gain of the system when $s \to 0$ is

$$\left.\begin{bmatrix}\tilde{v}_{fly1}\\ \tilde{v}_{fly2}\end{bmatrix}\right|_{steady\text{-}state,\ coupled} = \begin{bmatrix}0 & \frac{L_{cross}}{d^2T}\\ -\frac{L_{cross}}{d^2T} & 0\end{bmatrix}\begin{bmatrix}\tilde{i}_{dist1}\\ \tilde{i}_{dist2}\end{bmatrix}. \tag{2.15}$$

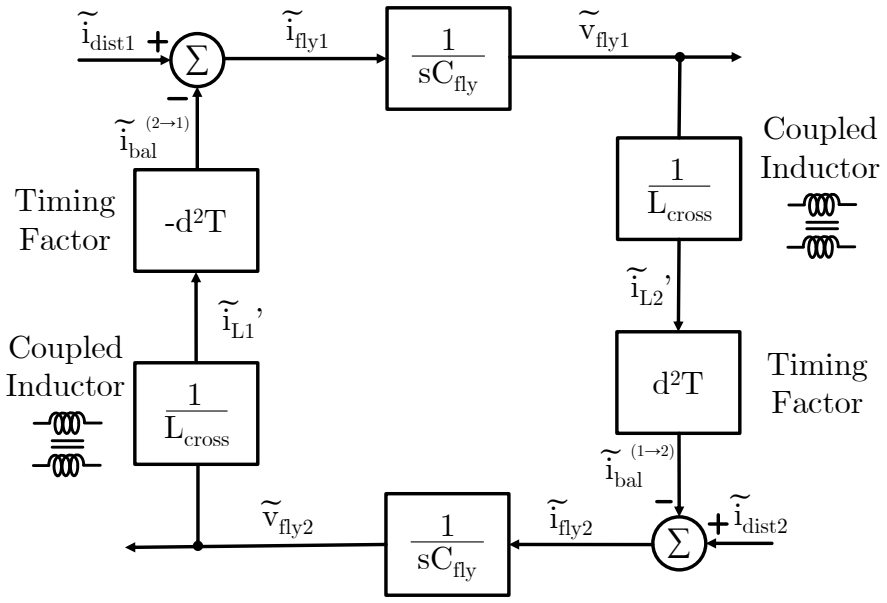


Figure 2.9: Detailed feedback balancing diagram of coupled inductor FCML converter where an imbalance voltage on phase #1 or #2 compensates for a disturbance on phase #2 or #1 respectively when $0 < d < \frac{1}{4}$.

The negative symbol is determined by the order of the switching order of phase #1 and phase #2 in a cycle. This equation confirms that the impact of coupled inductor balancing is only determined by L_{cross}, d, and T and is independent from resistance R_w.

We now compare the imbalances in the uncoupled (2.13) and coupled (2.15) cases. If the same disturbance is applied to both converters, the ratio of the steady-state imbalance voltage between the coupled and uncoupled converter when $0 < d < \frac{1}{4}$ is

$$\left| \frac{\tilde{v}_{\text{fly, coupled}}}{\tilde{v}_{\text{fly, uncoupled}}} \right| = \frac{L_{\text{cross}}}{d^2 T} \times \frac{\gamma}{Q_L^2 R_w}. \tag{2.16}$$

In a tightly coupled inductor design, L_{cross} is usually much smaller than $L_{\text{uncoupled}}$. In this case, the imbalance of the coupled inductor system is much smaller than the uncoupled system. As we seek to reduce converter losses by minimizing R_w and maximizing the quality factor of the inductor Q_L, the relative strength of coupled inductor balancing becomes more pronounced.

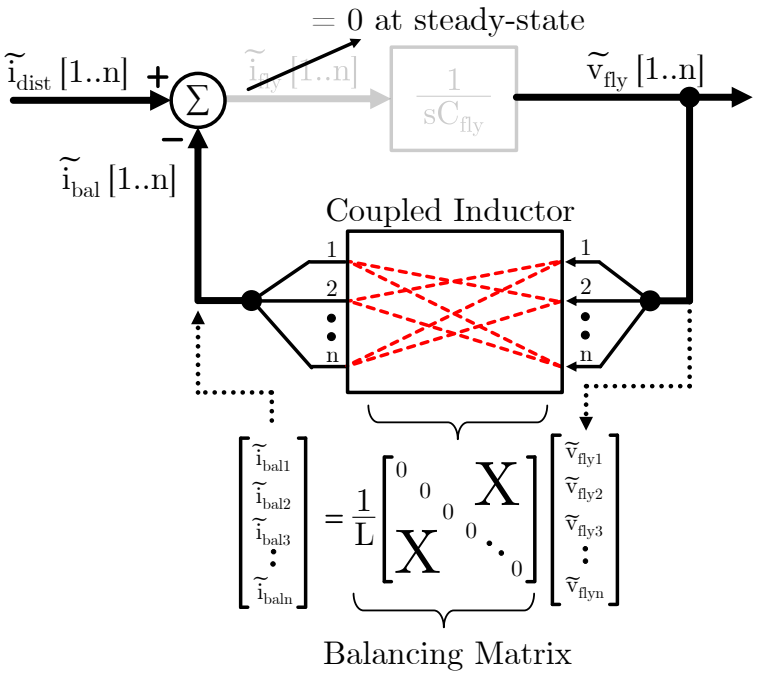


Figure 2.10: Generalized feedback balancing diagram for an FCML converter with an arbitrary number of flying capacitors.

2.4 A Generalized Modeling Framework for Steady-State Balancing Analysis

This section develops a generalized framework for analyzing coupled inductor balancing for converters with an arbitrary number of phases and levels. This model is used to determine the applicability and limitations of balancing with coupled inductors in multiphase FCML converters.

2.4.1 Feedback Model of Coupled Inductor Balancing for Arbitrary FCML Converter Size

First, we extend the feedback models in Section 2.3.3 to any FCML converter size. Consider a converter with M phases and $(K+2)$-levels with a total of $n = MK$ flying capacitors in the system. Fig. 2.10 shows the generalized feedback diagram. The bold connections are signal buses for all the n flying capacitor voltages and currents. With n flying capacitors, each flying capacitor voltage imbalance induces a current that balances up to $n-1$ other capacitors through the coupled inductors. This is represented by the balancing matrix in Fig. 2.10. The balancing matrix describes the effective balancing current or charge that is induced in every flying capacitor as a result of the imbalance voltages in all the other flying capacitors. The balancing matrix is important, because it determines whether or not the coupled inductors can counteract the disturbance

currents.

By inspection of Fig. 2.10, we define the following **multiphase FCML balancing criterion:** the converter is balanced if the flying capacitor imbalance voltages can balance an arbitrary set of disturbance currents. This criterion is met if the balancing matrix is full rank. Having a full-rank balancing matrix means that the system only has one unique periodic-steady-state and will not oscillate between two or more states. This property and the generalized feedback diagram are used throughout the rest of this chapter.

If the system is to reach a steady state with a persistent disturbance current ($\tilde{\mathbf{i}}_{\text{dist}}$) at each phase, the disturbance current in every capacitor needs to be canceled by the total cross-phase balancing current ($\tilde{\mathbf{i}}_{\text{bal}}$) introduced by the coupled inductors:

$$\tilde{\mathbf{i}}_{\text{bal}} + \tilde{\mathbf{i}}_{\text{dist}} = 0. \tag{2.17}$$

Assuming the system is periodic with T, eq. (2.17) can be rewritten in terms of charges instead of currents as

$$\mathbf{Q}_{\text{bal}} + \mathbf{Q}_{\text{dist}} = \mathbf{A}\tilde{\mathbf{v}}_{\text{fly}} + \mathbf{Q}_{\text{dist}} = 0, \tag{2.18}$$

where $\tilde{\mathbf{v}}_{\text{fly}}$ is a vector of all the flying capacitor voltage imbalances. The balancing matrix $\mathbf{A}$ relates the flying capacitor imbalance voltages to the resulting balancing charges on the other flying capacitors and depends on the switching order, duty cycle, and coupling ratio.. We can find the steady-state capacitor imbalances in terms of the disturbance charge if and only if $\mathbf{A}$ is invertible.

$$\tilde{\mathbf{v}}_{\text{fly}} = -\mathbf{A}^{-1}\mathbf{Q}_{\text{dist}}. \tag{2.19}$$

In summary, the balancing matrix $\mathbf{A}$ describes the amount of balancing charge induced in each phase by the others through the coupled inductor. If $\mathbf{A}$ is full rank, then an arbitrary disturbance can be canceled out by the coupled inductor and the system is balanced and will reach a steady-state computer by eq. (2.19).

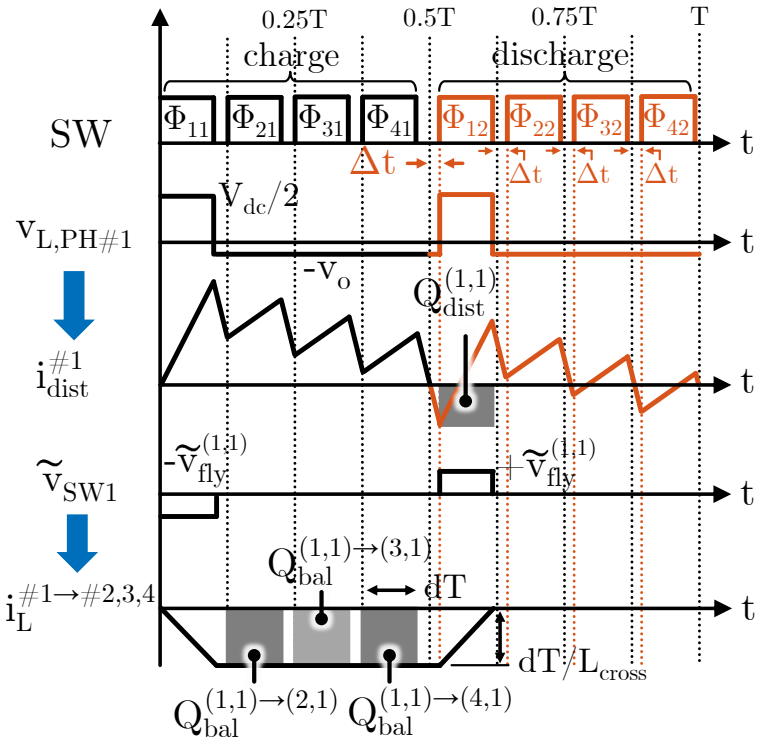


Figure 2.11: Switching waveforms of four-phase, three-level FCML converter with the second set of switches delayed by a disturbance. The disturbance charge caused by the delay and the balancing charge caused by the other flying capacitors must cancel out at steady-state.

2.4.2 Balancing with an Arbitrary Number of Phases

This section shows that an M-phase coupled inductor can balance the flying capacitors of any even number of three-level FCML converter phases. To prove this, we compute the balancing matrix and show that it is full rank. We begin with the case when the duty cycle is in the region $0 < d \leq \frac{1}{2M}$. First, we consider if the flying capacitor of phase #1 has a positive imbalance, $\tilde{v}_{\text{fly}}^{(1,1)}$. This imbalance is applied negatively and positively to the switch node once per period, as shown in Fig. 2.11 for a four-phase example. This induces an imbalance inductor current $i_{\text{L}}^{\#1\rightarrow\#2,\#3,\#4}$ in the other three phases. When the other three flying capacitors are connected, they receive a charge transfer labelled $Q_{\text{bal}}^{(1,1)\rightarrow(2,1)}$, $Q_{\text{bal}}^{(1,1)\rightarrow(3,1)}$, and $Q_{\text{bal}}^{(1,1)\rightarrow(4,1)}$. Therefore, the charge transfer induced by phase #1 in the other flying capacitors is

$$Q_{\text{bal}}^{(1,1)\rightarrow(m,1)} = -\frac{(dT)^2}{L_{\text{cross}}}\tilde{v}_{\text{fly}}^{(1,1)}, \tag{2.20}$$

for $m = 2, \ldots, M$. Thus, a positive voltage imbalance on flying capacitor (1,1) causes a uniform negative charge transfer on the other flying capacitors. We calculate the remaining entries of the balancing matrix in a similar way. All the flying capacitors cause the same charge transfer magnitude in the other phases; the only difference is the sign, which will be positive or negative depending on whether the target flying capacitor is in its charging or discharging phase. The resulting charge transfers are

$$Q_{\text{bal}}^{(m_\text{s},1)\rightarrow(m_\text{t},1)} = \begin{cases} -\frac{(dT)^2}{L_\text{cross}}\tilde{v}_\text{fly}^{(m_\text{s},1)} & m_\text{s} < m_\text{t} \\ +\frac{(dT)^2}{L_\text{cross}}\tilde{v}_\text{fly}^{(m_\text{s},1)} & m_\text{s} > m_\text{t} \\ 0 & m_\text{s} = m_\text{t} \end{cases}, \tag{2.21}$$

where $m_\text{s} = 1, \ldots, M$ is the "source" flying capacitor that is unbalanced, and $m_\text{t} = 1, \ldots, M$ is the "target" flying capacitor that receives a charge. From eq. (2.21), we write the complete balancing matrix that relates the imbalance voltages and balancing currents in matrix form

$$\mathbf{A} = \frac{(dT)^2}{L_\text{cross}} \underbrace{\begin{bmatrix} 0 & 1 & 1 & 1 & \cdots & 1 \\ -1 & 0 & 1 & 1 & \cdots & 1 \\ -1 & -1 & 0 & 1 & \cdots & 1 \\ -1 & -1 & -1 & 0 & \cdots & 1 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & -1 & -1 & \cdots & 0 \end{bmatrix}}_{\mathbf{X_{M\times M}}} \tag{2.22}$$

for an M-phase, three-level converter with $d < \frac{1}{2M}$. The main diagonal is zeros, since no flying capacitor induces a net charge transfer in itself. The remaining entries all have the same magnitude and sign determined by the switching order. The flying capacitor voltage imbalance will reach a steady state if $\mathbf{A}$ is invertible. As shown in Appendix III, $\mathbf{A}$ is invertible for an even M, and is non-invertible for an odd M.

Case Study: Time Delay in an Even M-Phase Converter

The prior analysis is applicable to any disturbance. As a case study of how the actual steady-state imbalances would be computed for a specific disturbance, we take a uniform time delay of the second set of switches (the pair further from the input side) of every phase for an even M-phase converter. This disturbance is illustrated in Fig. 2.11. Because of the time delay Δt, which might be caused by rise/fall times, signal mismatches, etc, the inductor current in each phase ramps down longer before the discharging phase of every flying capacitor. The current in phase #1, $i_L^{\#1}$, is shown as an example. This means that all the flying capacitors charge more than they discharge during every switching period, resulting in a persistent unbalancing current. The disturbance charge, shown by the shaded area under the $i_{\text{dist}}^{\#1}$ curve in Fig. 2.11, is

$$Q_{\text{dist}}^{(m,1)} = dT \times \frac{dV_{\text{dc}}}{L_l}\Delta t, \tag{2.23}$$

for $m = 1 \ldots M$ where L_l is the leakage inductance of the coupled inductor from the transformer model in Fig. 2.3. Therefore, the complete disturbance vector is

$$\mathbf{Q}_{\text{dist}} = dT\frac{dV_{\text{dc}}}{L_l}\Delta t \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \\ \vdots \end{bmatrix}_{M\times 1}. \tag{2.24}$$

We now plug the disturbance vector into eq. (2.19) to find the steady-state capacitor voltage imbalances are

$$\tilde{\mathbf{v}}_{\text{fly}} = \begin{bmatrix} \tilde{v}_{\text{fly}}^{(1,1)} \\ \tilde{v}_{\text{fly}}^{(2,1)} \\ \tilde{v}_{\text{fly}}^{(3,1)} \\ \vdots \\ \tilde{v}_{\text{fly}}^{(M,1)} \end{bmatrix} = -\mathbf{A}^{-1}\mathbf{Q}_{\text{dist}} = V_{\text{dc}}\frac{\Delta t}{T}\frac{L_{\text{cross}}}{L_l} \begin{bmatrix} 1 \\ -1 \\ 1 \\ \vdots \\ -1 \end{bmatrix}_{M\times 1}, \tag{2.25}$$

where the inverse of $\mathbf{A}$ is computed in Appendix III. The voltage imbalances with coupled inductor balancing are only dependent on the coupling coefficient and not on losses, since loss-based natural balancing is negligible. The magnitudes in all capacitors are equal and the signs are deter-

mined by the switching order. One half of the capacitors have positive voltage imbalance, while the other half have negative voltage imbalance. The steady-state imbalance is proportional to $\Delta t/T$ and M. The voltage imbalance also increases with the number of phases. A higher coupling ratio k leads to smaller steady-state voltage imbalances, and if the windings are perfectly coupled, i.e., $\mu \to +\infty$, the minimum steady-state voltage imbalance is

$$\tilde{\mathbf{v}}_{\text{fly}}\big|_{\text{tightly coupled}} \approx V_{\text{dc}} \frac{M\Delta t}{T} \begin{bmatrix} 1 \\ -1 \\ 1 \\ \vdots \\ -1 \end{bmatrix}_{1\times M}, \tag{2.26}$$

following from eq. (2.2). Note that for time delay disturbances, the voltage balancing is also independent of the power level of the FCML converter. For other disturbances, coupled inductor balancing can still be dependent on the load.

We now consider a more general time-shift disturbance when the second set of switches of every converter phase is time-shifted from the first set by Δt positively (lead) or negatively (lag), as in Fig. 2.11. Appendix III derives the best- and worst- case imbalances for this arbitrary time shift disturbance. In the worst case, all the time shifts are alternating direction and the disturbance vector is

$$\mathbf{Q}_{\text{worst-case}} = dT\frac{dV_{\text{dc}}}{L_l}\Delta t \begin{bmatrix} +1 \\ -1 \\ +1 \\ -1 \\ \vdots \end{bmatrix}_{M\times 1}, \tag{2.27}$$

and the largest flying capacitor imbalance is

$$\max\left(\tilde{\mathbf{v}}_{\text{fly}}\right)\big|_{\text{worst-case}} = \frac{(M-1)V_{\text{dc}}\Delta t}{T}\left(\frac{M-1}{k}+M\right). \tag{2.28}$$

The imbalance scales with M^2, meaning the balancing becomes weaker as M increases.

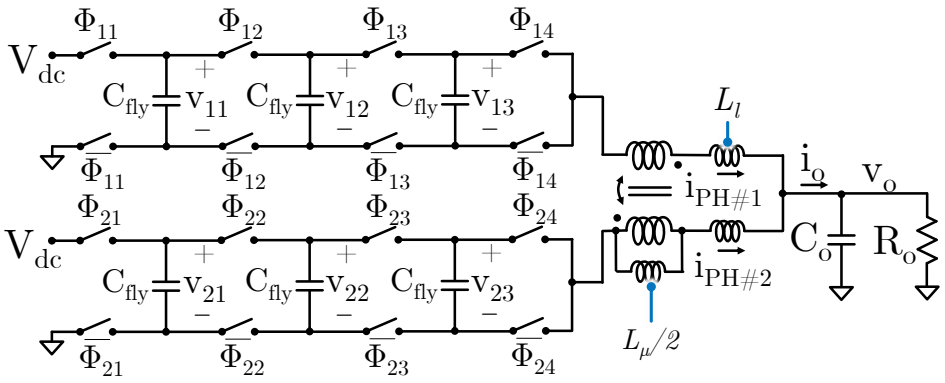


Figure 2.12: Schematic of two-phase, five-level FCML converter with coupled inductors. The flying capacitors are numbered by the second index $k = 1, 2, 3$, where $k = 1$ is closest to the input voltage source.

2.4.3 Balancing with an Arbitrary Number of Levels

This section shows that coupled inductors can balance FCML converters with any finite number of levels. We prove this by computing the balancing matrix for a $(K + 2)$-level converter and showing that it is full rank.

Fig. 2.12 shows a two-phase, five-level converter with switching waveforms in Fig. 2.13 for $d < \frac{1}{2(K+1)}$ as an example. The steps required to prove the balancing capabilities of a $(K+2)$-level converter are similar to Section 2.4.2. Each flying capacitor imbalance voltage causes balancing charge transfers in the other flying capacitors. The balancing matrix (derived in Appendix IV) is

$$\mathbf{A}_{\text{(K+2)-levels}} = \begin{bmatrix} 0 & \alpha & \beta & 0 & 0 & \cdots & 0 \\ -\alpha & 0 & \alpha & \beta & 0 & \cdots & 0 \\ -\beta & -\alpha & 0 & \alpha & \beta & \cdots & 0 \\ 0 & -\beta & -\alpha & 0 & \alpha & \cdots & 0 \\ 0 & 0 & -\beta & -\alpha & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & 0 & \cdots & 0 \end{bmatrix}, \tag{2.29}$$

where $\alpha = \frac{(dT)^2}{L_{\text{cross}}}$ and $\beta = \frac{(dT)^2}{2L_{\text{same}}}$. The *same* inductance L_{same} appears because there are multiple flying capacitors in the same phase that induce balancing currents in each other. The size is $2K \times 2K$ because each phase has K flying capacitors. The vector of flying capacitor voltages correspond-

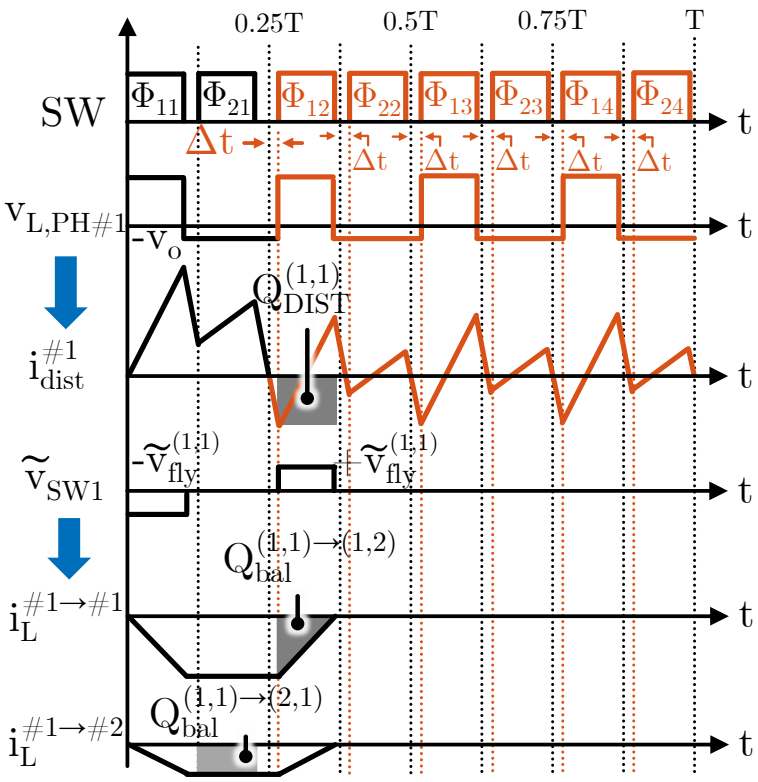


Figure 2.13: Switching waveforms of two-phase, five-level FCML converter with time delay disturbance. An imbalance on capacitor #1 of phase #1 will cause a balancing charge on capacitor #2 of phase #1 and capacitor #1 of phase #2.

ing with eq. (2.29) is

$$\mathbf{v} = \begin{bmatrix} v_{\text{fly}}^{(1,1)} & v_{\text{fly}}^{(2,1)} & v_{\text{fly}}^{(1,2)} & v_{\text{fly}}^{(2,2)} & \cdots & v_{\text{fly}}^{(1,K)} & v_{\text{fly}}^{(2,K)} \end{bmatrix}^{\text{T}}. \tag{2.30}$$

As proven in Appendix IV, $\mathbf{A}_{\text{(K+2)-levels}}$ is invertible for any finite number of levels if the coupled inductors are fully coupled ($L_{\text{same}} = L_{\text{cross}}$). In Section 2.5, we treat cases with other duty cycles and phase counts.

Case Study: Time Delay in a Two-Phase, Five-Level Converter

As an example of how the actual steady-state imbalances would be computed for a specific disturbance, we analyze a uniform time delay disturbance between every pair of switches and the pair closest to the input voltage source for the five-level converter. Fig. 2.13 shows the inductor current in phase #1 because of this disturbance. The shaded area shows the disturbance charge that would result on flying capacitor (1,1). As with Section 2.4.2, we compute the disturbance charge on every capacitor (a total of six). At steady-state, eq. (2.19) yields the steady-state flying capacitor voltage imbalances

$$\tilde{\mathbf{v}}_{\text{fly}} = \begin{bmatrix} \tilde{v}_{\text{fly}}^{(1,1)} \\ \tilde{v}_{\text{fly}}^{(2,1)} \\ \tilde{v}_{\text{fly}}^{(1,2)} \\ \tilde{v}_{\text{fly}}^{(2,2)} \\ \tilde{v}_{\text{fly}}^{(1,3)} \\ \tilde{v}_{\text{fly}}^{(2,3)} \end{bmatrix} = -\mathbf{A}^{-1}\mathbf{Q}_{\text{dist}} \approx V_{\text{dc}} \times \frac{\Delta t}{T} \begin{bmatrix} 3 \\ -3 \\ 2 \\ -2 \\ 1 \\ -1 \end{bmatrix}, \tag{2.31}$$

if we take the coupled inductors as tightly coupled with $L_{\text{cross}} = L_{\text{same}}$. Again, the flying capacitor imbalances have magnitudes and signs determined by the switching order. Like in the M-phase case, the imbalance depends on the relative severity of the time delay compared to the period.

2.4.4 Balancing with Partially Coupled Inductors

So far, we have assumed the inductors are fully coupled and that the converter losses are negligible. In this section, we show that tightly coupled inductors minimize the imbalance and illustrate

the effect that losses and natural balancing have in conjunction with coupled inductor balancing.

In a practical circuit with losses, natural balancing and coupled inductor balancing act simultaneously, and the combination of the balancing effects determines the steady-state flying capacitor voltages. If the inductors are uncoupled, there is only natural balancing. If the inductors are very tightly coupled, natural balancing is overshadowed by the much stronger coupled inductor balancing effect. In terms of the feedback diagrams in Section 2.3, coupled inductor and natural balancing are two parallel feedback paths, and the stronger path will exert the most prominent balancing effect.

Fig. 2.14 illustrates how the strength of coupled inductor balancing increases as the coupling ratio $\frac{L_\mu}{L_l}$ is increased. As the coupling ratio increases, coupled inductor balancing becomes stronger. Natural balancing, meanwhile, has constant strength since the losses remain the same. For very loose or no coupling, natural balancing dominates. As coupling increases, coupled inductor balancing overtakes natural balancing and reaches a much higher total balancing strength, which leads to smaller voltage imbalances at steady-state. When the coupling ratio becomes very high, the balancing strength reaches the limits derived in sections 2.4.2 and 2.4.3, where we assumed fully coupled inductors.

Case Study: Partially Coupled Four-Phase Converter

In this case study, we simulate the flying capacitor imbalances of a four-phase converter as we vary the inductors from being uncoupled to very tightly coupled. Fig. 2.15 shows the simulation results of a four-phase, three-level FCML converter with a $\Delta t = 2$ ns delay as the disturbance, $f_{sw} = 500$ kHz, $C_{\text{fly}} = 1\ \mu$F, $L_l = 300$ nH and $d = 0.125$ as a function of the coupling ratio $\frac{L_\mu}{L_l}$. At very low coupling ratios, the inductors are almost uncoupled and the flying capacitor voltages are determined primarily by natural balancing. As the coupling ratio increases, the strength of coupled inductor balancing increases, which causes the flying capacitor imbalances to decrease. In fact, the imbalance voltages decrease within the envelope outlined by the dotted lines from the predicted imbalances from Section 2.4.2. At very high coupling ratios, the flying capacitor

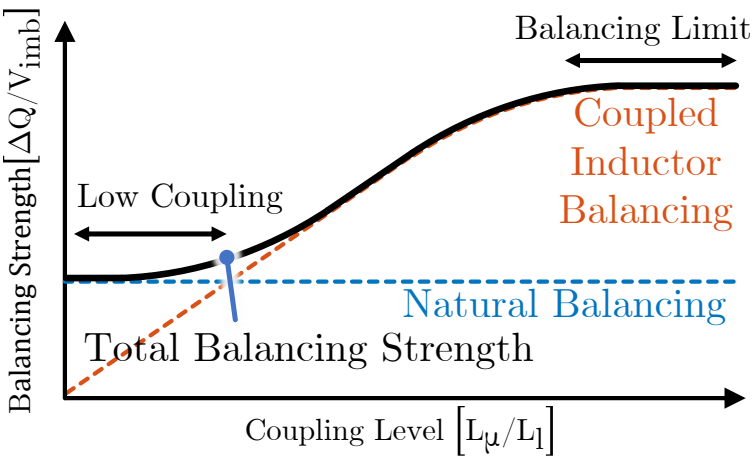


Figure 2.14: Combination of natural and coupled inductor balancing. As the coupling level increases, coupled inductor balancing becomes stronger than natural balancing and dominates the balancing characteristics. Very tightly coupled inductors reach the maximum limit of balancing strength.

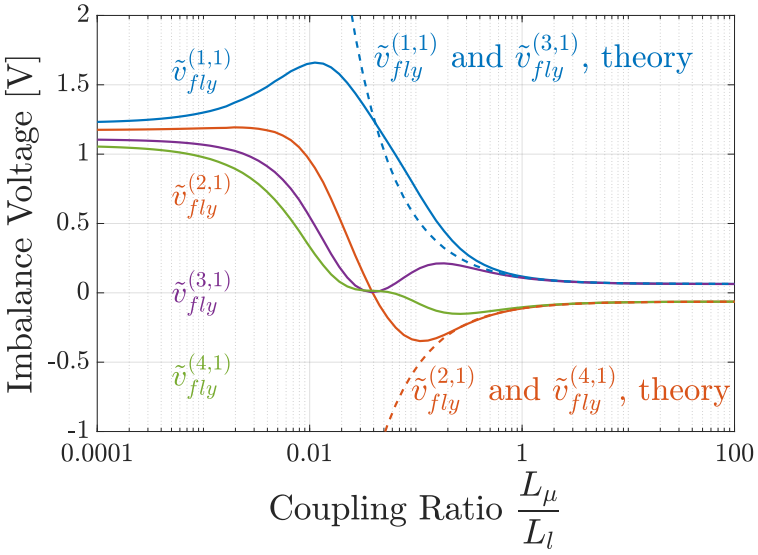


Figure 2.15: Simulated flying capacitor voltage imbalances of a four-phase, three-level converter plotted vs. the coupling ratio with $V_{\text{dc}} = 16$ V, $f_{sw} = 500$ kHz, a $\Delta t = 2$ ns delay, and $d = 0.125$. As the coupling ratio increases, the strength of coupled inductor balancing increases and reduces the imbalance.

imbalances are minimized.

With a low to moderate coupling ratio (L_μ/L_l between about 0.01 and 1), the strength of the balancing mechanisms is comparable. This explains how $v_{\text{fly}}^{(1,1)}$ initially increases under the influence of multiple balancing factors which lead it to compensate for the other phases with a high imbalance. Since this could negatively impact one of the phases even though the others are improved, it is advisable to have a high coupling ratio such that coupled inductor balancing dominates natural balancing. This minimum depends on the application, but Fig. 2.15 shows that even a modest coupling ratio of $\frac{L_\mu}{L_l} = 1$ yields most of the balancing benefits.

2.5 Singularities where Coupled Inductor Balancing Fails

Section 2.4 derives a mathematical framework that proves the balancing capabilities of coupled inductors. The only theoretical limitations found so far are the requirement of an even number of phases, a moderate coupling ratio, and the fact that balancing may become weaker as the number of flying capacitors increases. However, these derivations assume perfectly coupled inductors and only certain duty cycle regimes. In this section, we consider all operating conditions and prove that coupled inductors balance FCML converters for almost all duty cycles and coupling ratios. In doing so, we also find point singularities where coupled inductor balancing fails if there are more than two phases or three levels. We predict the location of these singularities and show how they place theoretical limits on the number of balanced phases, levels, and the required coupling ratio.

2.5.1 Duty Cycle Singularities with More Than Two Phases

While coupled inductors can balance any even number of three-level phases for $d < \frac{1}{2M}$ as shown in Section 2.4.2, we must also treat the other duty cycle regions. The procedure for determining the balancing capability in any duty cycle region is similar to the approach in Section 2.4: i) compute the balancing matrix, ii) compute the determinant, and iii) find the conditions, if any, for which the determinant is zero.

In Appendix V, we note that if the phase converter operation is symmetric and every phase has

Table 2.2: Number of Singularities in Multiphase Three-level FCML Converter Balancing Matrix for $0 < d \leq 0.5$, with symmetry for the $0.5 < d < 1$ range

M	Duty cycle regime i									
	1	2	3	4	5	6	7	8	9	10
2	0	0								
4	0	0	2	0						
6	0	0	1	1	0	0				
8	0	0	2	0	0	0	4	0		
10	0	0	2	1	0	0	0	1	0	0

the same phase shift, the balancing matrix is skew-symmetric. This property can be used to show that **coupled inductor balancing almost always works for any even number of phases, any number of levels, and any duty cycle:**

$$|\mathbf{A}| \neq 0 \quad \forall \quad d \in (0,1), d \notin \mathcal{D}. \tag{2.32}$$

Equation (2.32) asserts that the balancing matrix has nonzero determinant and the converter is balanced for all cases except for a finite set of duty cycle singularities $\mathcal{D}$ with size $n(\mathcal{D}) \leq M^2K(K+1)$.

This analysis reveals that coupled inductor balancing fails at specific duty cycles depending on the number of phases and levels. These singularities exist because the elements of the balancing matrix are functions of the d and there are some values of d for which the balancing matrix is singular. We can find these values by solving for the roots of the determinant. Table 2.2 lists the number of singularities for three-level converters and the duty cycle regime i they occur in, where the duty cycle is $\frac{i-1}{M(K+1)} < d \leq \frac{i}{M(K+1)}$. There are no singularities for the two-phase converter, but the number of singularities increases as the number of phases increases, putting a theoretical limitation on the number of phases and levels that can be balanced.

Using multiple two-phase coupled inductors instead of a single multiphase coupled inductor can improve balancing performance. This is because there are no duty cycle singularities with two-phase coupled inductors, as proven in this section, combined with the analysis in section 2.4.2 and equations (2.25) and (2.28) showing that the balancing strength decreases with increasing phases. Using multiple two-phase coupled inductors may lead to higher ripple or larger

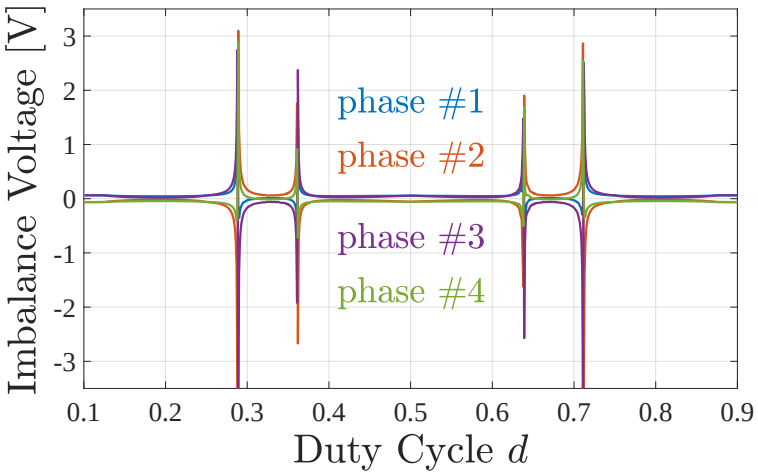


Figure 2.16: Simulated flying capacitor voltage imbalances of a four-phase converter with $V_{\text{dc}} = 16$ V, $f_{sw} = 500$ kHz, and a time delay disturbance of $\Delta t = 2$ ns on each phase. There are singularities in the balancing matrix at certain duty cycles, resulting in diverging capacitor voltages.

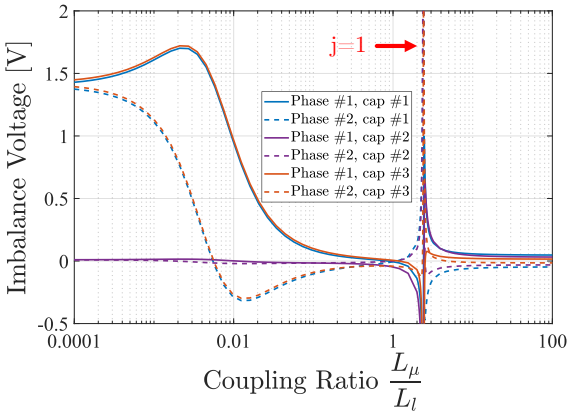
size compared to one multiphase coupled inductor. [26].

Case Study: Four-phase Converter Singularities

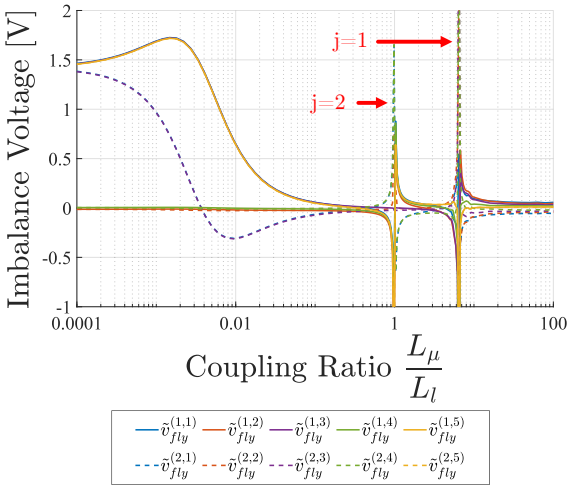
We now consider a numerical example to illustrate the impact of the duty cycle singularities. In Appendix V, we derive the balancing matrix of the four-phase, three-level converter and numerically compute the duty cycles at which the balancing matrix is singular, finding two such duty cycles at $\mathcal{D} = \{0.2836, 0.3629\}$, which are both in the $\frac{1}{4} < d \leq \frac{3}{8}$ region. Theoretically, coupled inductor voltage balancing is not effective at these two duty cycles. Fig. 2.16 shows the simulated imbalances with a $\Delta t = 2$ ns delay, $f_{sw} = 500$ kHz, $C_{\text{fly}} = 1$ μF, and $L_\mu / L_l = 100$. The coupled inductors balance the four flying capacitor voltages for most duty cycles, but divergence can be observed at the predicted duty cycle points, along with their mirrored counterparts across the $d = 0.5$ axis. In a practical converter, there are asymmetries, losses, and non-idealities that could reduce the divergence at the singularity points.

2.5.2 Coupling Ratio Singularities with More Than Three Levels

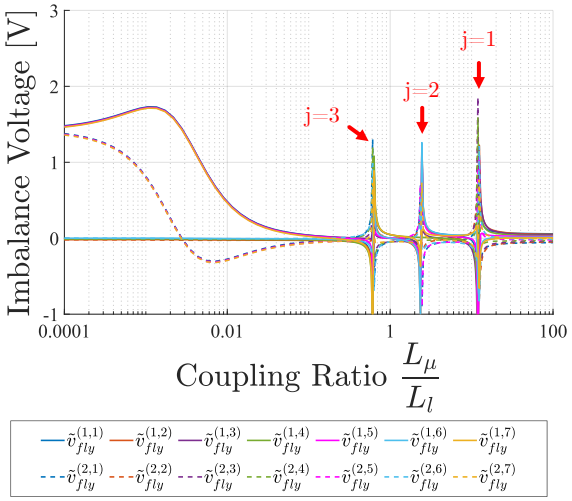
In Section 2.4.3 and 2.4.4, we showed that fully coupled inductors can balance FCML converters with any finite number of levels, and that the balancing strength tends to improve as the coupling ratio is increased. We now treat partially coupled inductors and find that balancing works for



(a)



(b)



(c)

Figure 2.17: Simulated flying capacitor imbalance voltages of a two-phase FCML converter with (a) five, (b) seven, or (c) nine levels. The simulations use $V_{\text{dc}} = 16$ V, $\Delta t = 2$ ns, $f_{sw} = 500$ kHz, $L_l = 300$ nH and $d = \frac{1}{2(K+1)}$. As the number of levels increases, the number of coupling ratio singularities in the balancing matrix, annotated by index j from eq. (2.33), increases.

almost all coupling ratios except at specific coupling singularities.

To find the coupling singularities, we use the same procedure of computing the balancing matrix and finding the conditions where its determinant is zero, except we find roots of the coupling ratio $\frac{L_{\text{same}}}{L_{\text{cross}}}$ instead of the duty cycle. **Coupled inductor balancing works for almost all cases except for a finite number of singular coupling ratios.** It is not only important to have a high coupling ratio to maximize balancing strength, but also to avoid coupling singularities that can impact the converter's robustness. To illustrate the coupling ratio restrictions, we turn to a case study of two-phase multilevel FCML converters.

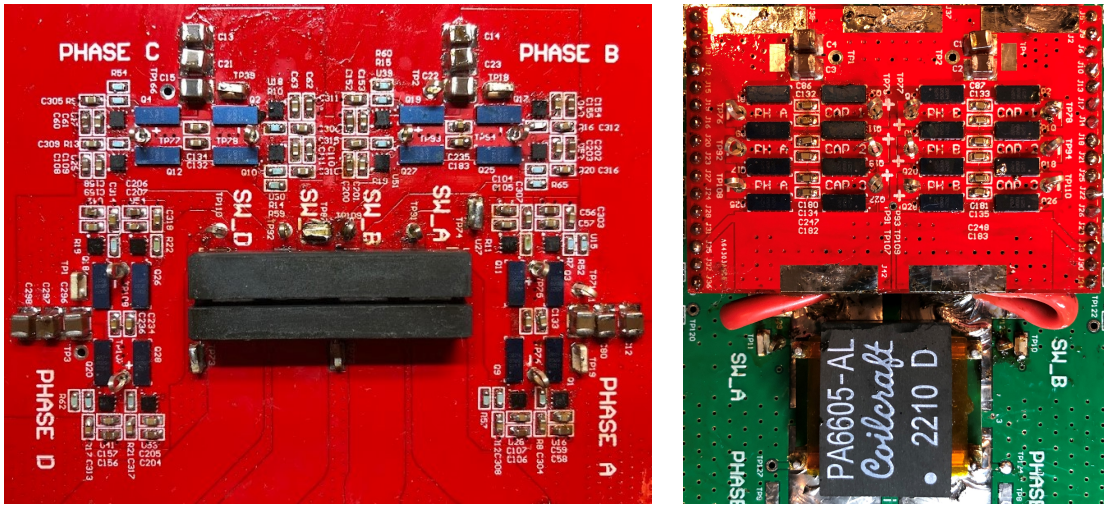
Case Study: Coupling Singularities of a Two-Phase Converter

Let us consider a two-phase converter with $d = \frac{1}{2(K+1)}$ and partial coupling. In this case study, we treat the duty cycle as fixed and vary the coupling ratio. Fig. 2.17 shows the simulated imbalances with a varying coupling ratio for five-, seven-, and nine-level converters. The imbalances generally follow the same pattern as in the four-phase case, with reducing imbalance as coupled inductor balancing strengthens, and the even-numbered capacitors tend to stay well-balanced throughout [46, 59]. However, there are point singularities at certain coupling ratios, with more singularities as the number of levels increases.

As derived Appendix IV, this case has explicit solutions for the locations of the singularities. If we let the coupling ratio be $x = \frac{L_{\text{same}}}{L_{\text{cross}}} = \frac{L_\mu}{(M-1)L_l+L_\mu} = \frac{\mu}{M-1+\mu}$ where $\mu = \frac{L_\mu}{L_l}$, the singularities are at

$$x_j = \cos\left(\frac{j}{K+1}\pi\right) \tag{2.33}$$

for $j = 1, \ldots K$. In the simulation, the flying capacitor voltages diverge at exactly these predicted roots; for example, the five-level converter has a predicted root at $x_1 = \frac{1}{\sqrt{2}}$, which corresponds to a coupling ratio of approximately $\frac{L_\mu}{L_l} \approx 2.41$. Eq. (2.33) also shows that the number of coupling singularities increases as the number of levels increases. The largest singularity, which occurs at $j = 1$, approaches $x_1 \to 1$ as $K \to \infty$. As the number of levels increases, the required coupling ratio also increases.



(a) (b)

Figure 2.18: (a) A four-phase, three-level FCML converter with off-the-shelf Eaton four-phase coupled inductor and (b) a two-phase, five-level FCML converter with off-the-shelf Coilcraft PA6605-AL inductor.

Table 2.3: Circuit Parameters of the FCML Prototype

Parameter/Component	**Value**
f_{sw}	500 kHz
V_{dc}	16 V
C_{fly}	1206 10 μF $\times$ 4
Custom Coupled Inductor L_l	192 nH
Custom Coupled Inductor L_μ	7.44 uH
Off-the-shelf Coupled Inductor	Eaton CL1108-4-50TR-R
Two-phase Coupled Inductor	Coilcraft PA6605-AL
Discrete Inductor	Coilcraft XAR7030-222MEB
Switches	EPC2024
Controller	TMS320F28379D

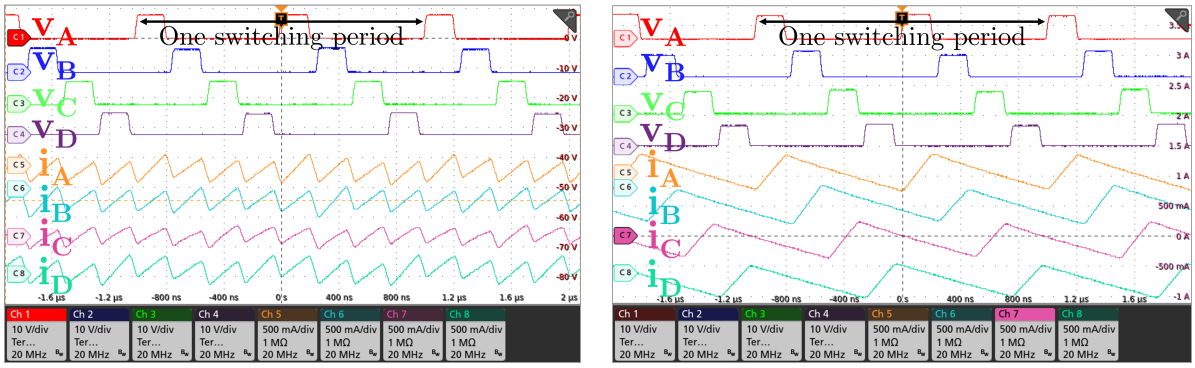
2.6 Experimental Verification

The theoretical predictions are verified using FCML converters with two or four phases and between three and five levels. Fig. 2.18 shows the two-phase, five-level and four-phase, three-level boards. The prototypes have the component values shown in Table 2.3, with the five-level converter having a lower switching frequency of 50 kHz due to gate driving limitations. To compare coupled inductor balancing to natural balancing, four inductors are used: discrete 2.2 μH inductors, an off-the shelf Eaton CL1108-4-50TR-R four-phase coupled inductor with $\frac{L_\mu}{L_l} = 2.66$, a custom four-phase coupled inductor with $\frac{L_\mu}{L_l} = 38.9$, and an off-the-shelf Coilcraft PA6605-AL two-phase coupled inductor with $\frac{L_\mu}{L_l} = 38.5$, which all have sufficient steady-state inductance for low ripple. The flying capacitors are rated for 50 V and have a class II X8L dielectric. The capacitances are selected to have small voltage ripple with the given load and switching frequency. At the selected input voltage, the capacitance varies around 10% for different dc biases in the five-level converter. If a higher input voltage is used, the effect of dc bias on different flying capacitors should be considered in a higher order converter.

The operating waveforms of the four-phase converter at $d = 0.1$ are shown in Fig. 2.19 with the (a) tightly coupled $\left(\frac{L_\mu}{L_l} = 38.9\right)$ inductors and (b) discrete inductors. Due to the three-level FCML structure and interleaving with coupled inductors, the effective ripple frequency is multiplied by eight. This considerably reduces the ripple amplitude.

The inductors compared in these experiments are selected to have similar ripple, as shown in Fig. 2.20. Because of this, the coupled inductors have a much lower leakage inductance of $L_l = 192$ nH compared to the discrete inductance of 2.2 μH. Therefore, the coupled inductor converter will have a much faster transient response, allowing it to respond to load transients more effectively [5]. Despite this, the coupled inductor converter still has lower ripple due to ripple cancellation at more duty cycles. Fig. 2.21 shows the converter efficiency being improved by coupled inductors.

To verify the balancing performance, a time delay of one set of switches between -40 ns and +40 ns is introduced using the digital controller. Fig. 2.22 shows the measured flying capacitor



(a) (b)

Figure 2.19: Measured switching waveforms of four-phase, three-level FCML converter with (a) coupled inductors and (b) discrete inductors. Because of the coupled inductors, the ripple frequency is four times higher with coupled inductors than discrete inductors.

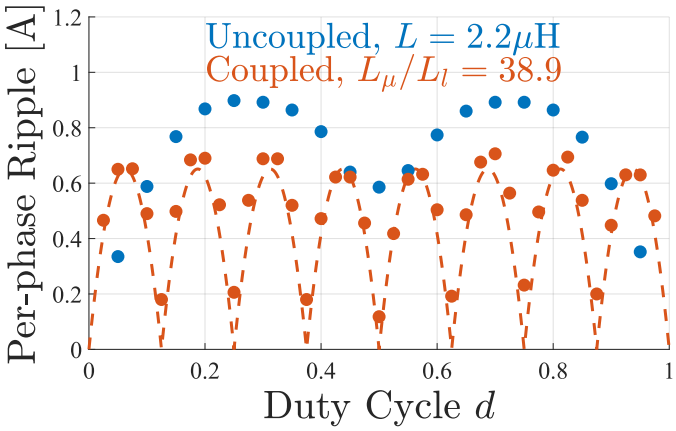


Figure 2.20: Measured per-phase current ripple average of the four phases. The inductors are chosen to have similar maximum ripple. Despite this, the coupled inductors generally have significantly lower ripple due to additional ripple cancellation points, matching well with the theoretical ripple shown by the dotted line. The uncoupled inductor ripple does not cancel at $d = 0.5$ due to flying capacitor voltage imbalances, even with no disturbances.

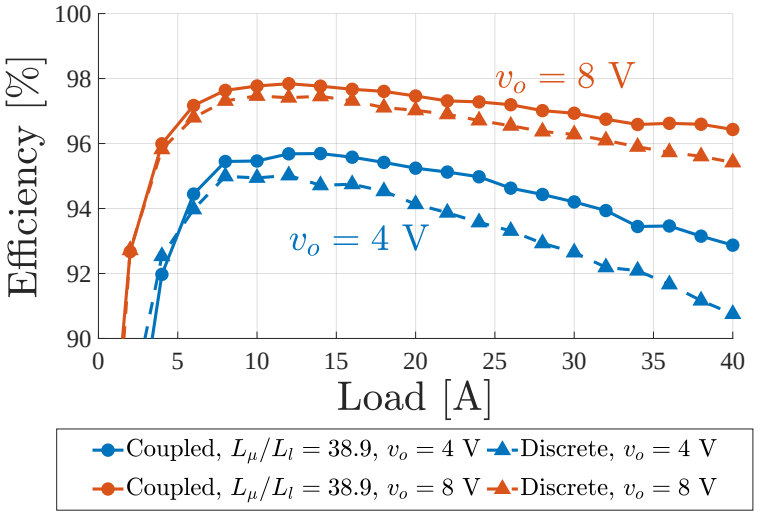


Figure 2.21: Measured converter efficiency at $v_o = 8$ V and $v_o = 4$ V, demonstrating coupled inductor efficiency improvements.

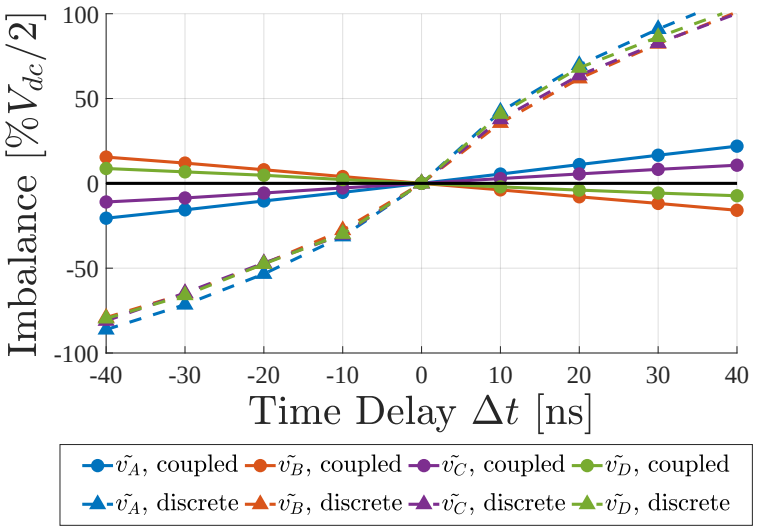


Figure 2.22: Flying capacitor voltage imbalance as a function of the time delay Δt at $d = 0.125$. With coupled inductors, the imbalance scales linearly with Δt, as predicted in eq. (2.25), and are much smaller with coupled inductors.

voltage imbalances of the four-phase, three-level converter at $d = 0.125$ as a function of the delay magnitude. The coupled inductors balance the flying capacitors much better than natural balancing, which reduces the voltage stress, ripple, and distortion.

Coupled inductor balancing improves as the coupling ratio increases, as shown in Fig. 2.23. In these plots, the imbalance is plotted across the duty cycle range for a time delay of $\Delta t = 10$ ns. With uncoupled inductors (a), the imbalances are large and reach an absolute maximum of 3.328 V. With the tightly coupled custom inductors (c), the imbalance is consistently limited to 0.559 V across the duty cycle range. With the off-the-shelf coupled inductors (b), which have a coupling ratio between the other two of $\frac{L_\mu}{L_l} = 2.66$, the balancing is less effective. The absolute maximum imbalance is 1.143 V, which is still considerably reduced compared to the results with discrete inductors.

As shown in Section 2.4.2, coupled inductor balancing becomes weaker and less reliable as the number of coupled inductor phases increases. However, these experiments show that a single four-phase coupled inductor is still suitable for balancing a four-phase converter. It is also possible to use two two-phase coupled inductors instead, which is the most reliable configuration. Fig. 2.23(d) shows the imbalances with two two-phase coupled inductors with $\frac{L_\mu}{L_l} = 38.5$ coupling phase #1 with phase #2 and phase #3 with phase #4.

Fig. 2.24 shows the measured imbalances of a four-phase, three-level converter where one complimentary pair of switches is phase shifted by 8° from ideal. The capacitor voltages are generally kept well balanced but do spike at four duty cycle points. These spikes coincide exactly with the singularities for a four-phase converter predicted in Section 2.5 to occur at $\mathcal{D} = \{0.2836, 0.3629\}$ and the corresponding points across the $d = 0.5$ axis. This experiment verifies both the existence of multiphase singularities and the validity of the balancing matrix approach for predicting their locations.

Fig. 2.25 shows the measured voltage imbalances of a two-phase, five-level converter with a time delay of $\Delta t = 300$ ns applied to each phase. A larger time delay is used to emphasize the imbalance since the switching period is longer. The coupled inductors keep the flying capacitors

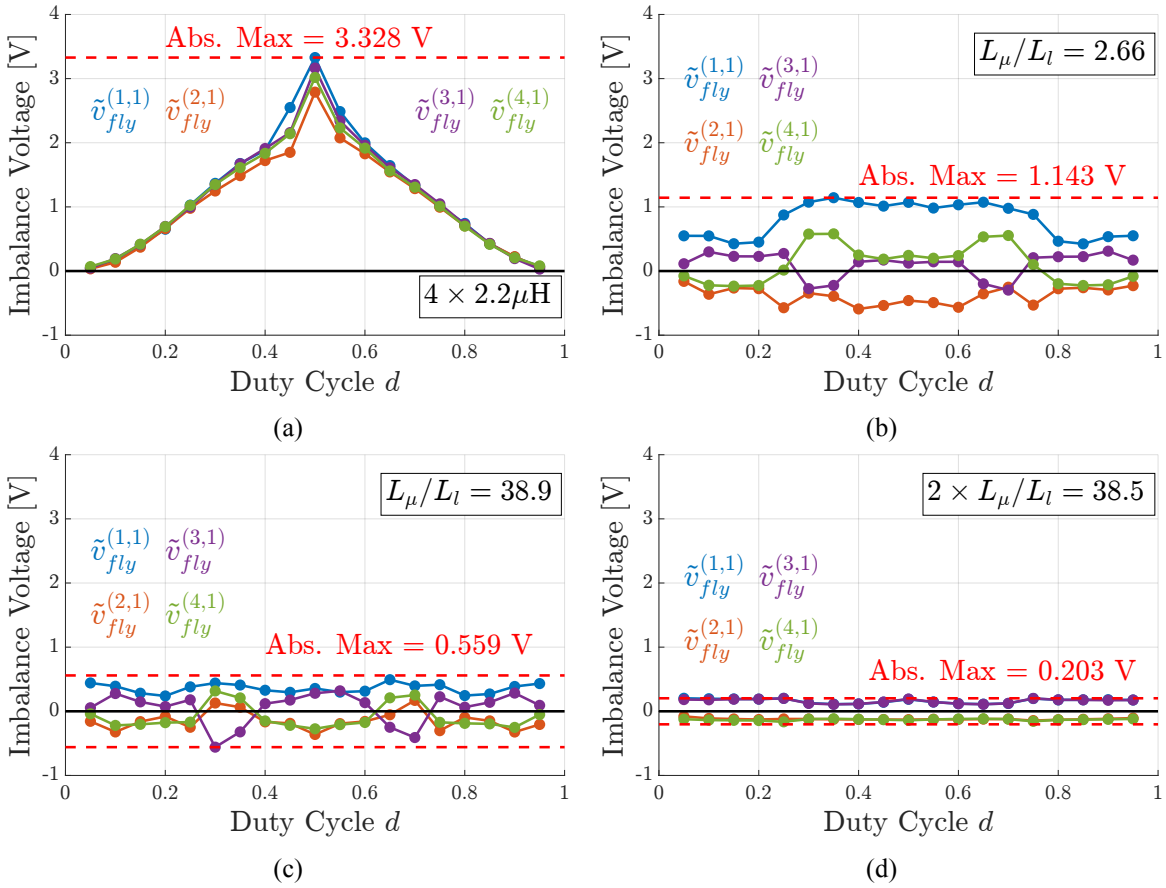


Figure 2.23: Flying capacitor voltage imbalances with constant time delay $\Delta t = 10$ ns and (a) four discrete 2.2 μH inductors, (b) off-the-shelf four-phase coupled inductors with $\frac{L_\mu}{L_l} = 2.66$, (c) custom four-phase coupled inductors with $\frac{L_\mu}{L_l} = 38.9$, and a pair of two-phase coupled inductors with $\frac{L_\mu}{L_l} = 38.5$. The input voltage is $V_{\text{dc}} = 16$ V.

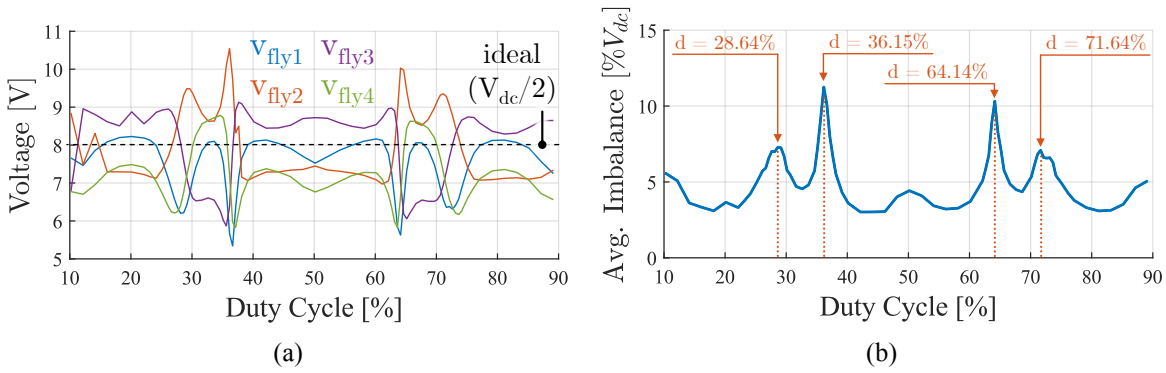


Figure 2.24: (a) Flying capacitor voltages of the four-phase converter kept well-balanced with a 8° phase shift on one complimentary pair of switches and a 6 A load. (b) Singularities of the four-phase converter at the theoretically predicted duty cycles.

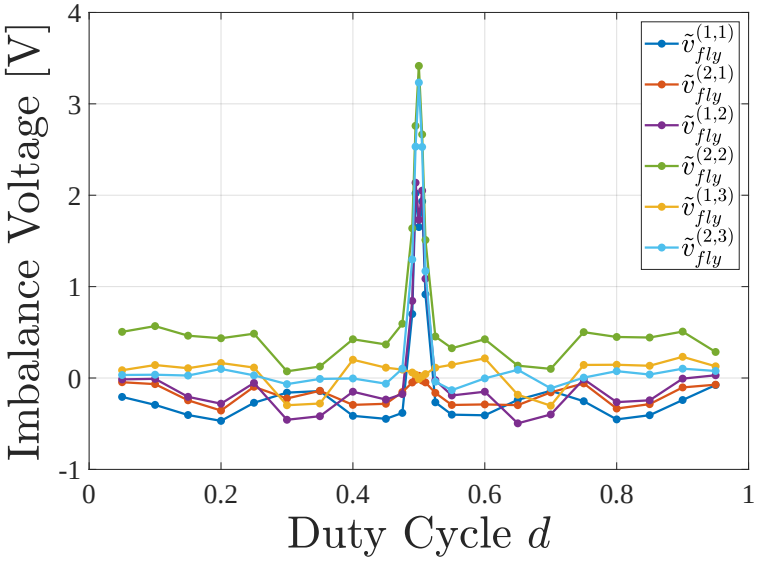


Figure 2.25: Flying capacitor voltage imbalances of two-phase, five-level converter with $V_{dc} = 16$ V and time delay $\Delta t = 300$ ns unbalancing the flying capacitors.

balanced for most duty cycles, but they diverge at $d = 0.5$. This is a nominal conversion ratio where the five-level converter is intrinsically imbalanced and another balancing mechanism is needed.

Fig. 2.26 verifies the balancing performance across load. Coupled inductor balancing maintains similar balancing performance at both high and low loads, making it applicable to a variety of operating conditions. Fig. 2.27 verifies that coupled inductor balancing functions well for a variety of randomized phase shift disturbances, both positive and negative, on all switches. A random phase shift between ±7°, equivalent to ±40 ns, is applied to all of the switches on the

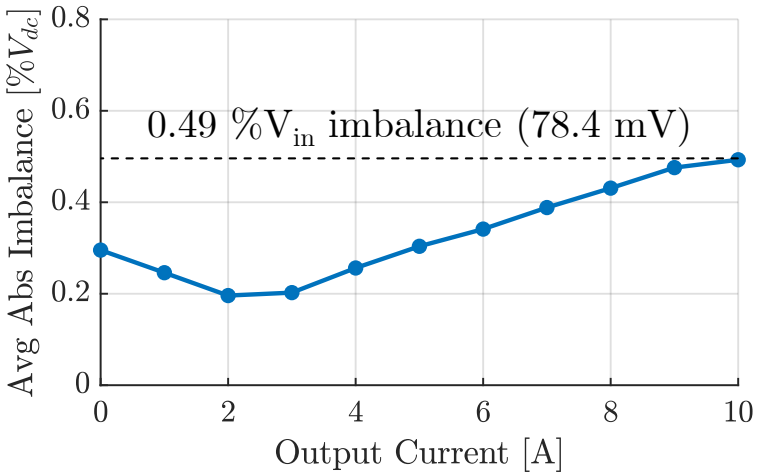


Figure 2.26: Average absolute flying capacitor voltage imbalance for four-phase, four-level FCML converter across output load at $d = 0.25$ and $V_{\text{dc}} = 16$ V.

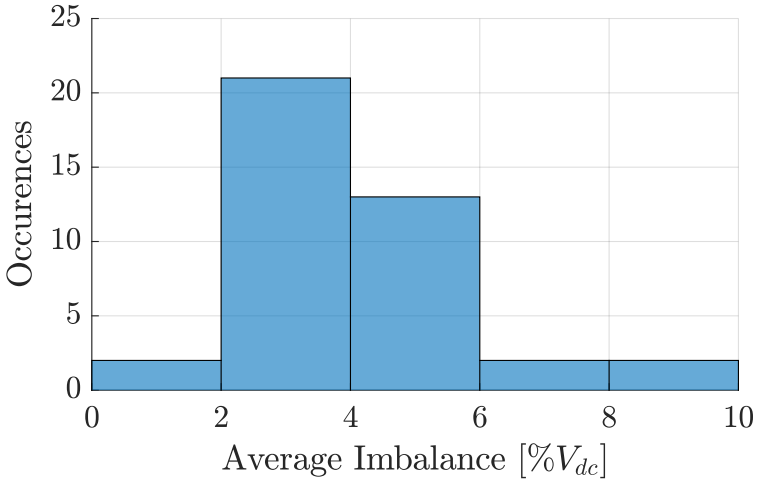


Figure 2.27: Histogram of average absolute imbalances with random phase shift disturbances on all switches between $\pm 7° \equiv 40$ ns at $f_{sw} = 490$ kHz and a 5 A load.

four-phase, four-level converter. Very large disturbance magnitudes are used to emphasize the imbalance. In a practical circuit, the disturbances would likely be smaller.

2.7 Comparison with Other Balancing Techniques and Design Guidelines

Having explained the fundamental mechanism of coupled inductor balancing, we can now compare its strengths and weaknesses to other common balancing techniques. Table 2.4 compares the impact of each method on voltage balancing, size, current ripple, loss, and complexity. Although converters with an even number of levels are less sensitive [59], natural balancing [34]

Table 2.4: Comparison of FCML Voltage Balancing Techniques

	Coupled Inductor	Natural Balancing	Active Balancing	Even-level Switching
References	[64–66, 68]	[34–37]	[39, 58]	[32, 46]
Balancing Strength	Strong	Weak	Strong	Depends
Steady-State	Yes	Yes	Yes	Partially
Transient	Faster	No change	Depends	No change
Reliant on Losses	No	Yes	No	No
Applicability	Even # phases, any # levels	Any # levels	Any # levels	Even # levels
Inductor Size	Reduced	No change	No change	No change
Current Ripple	Reduced	No change	No change	No change
Load Dependence	No	Yes	Sometimes	No
Passivity	Passive	Passive	Active	Passive

has the general drawback of variability and dependence on losses, and is not typically relied on as a sole balancing method. Active balancing [39] uses measurement or estimation of the flying capacitor voltages and active control to balance them. This is a very flexible and robust technique that can handle many unbalanced structures. Additionally, active balancing can, with appropriate feedback control, force the steady-state imbalance to be zero, while passive balancing methods like coupled inductors will still have a nonzero, albeit small, remaining imbalance. However, it does have the disadvantage of needing additional hardware and control for every flying capacitor that must be balanced, and the control bandwidth is limited. Additionally, some active balancing techniques rely on the load current to balance the capacitors and do not work at light load, while coupled inductor balancing works independently of the load current.

Compared to other existing balancing approaches, coupled inductor balancing offers the following advantages: i) Strong voltage balancing without the need to rely on converter losses or complex sensing and control hardware, ii) Good scaling to higher-order multilevel multiphase converters where more capacitors must be balanced, or high bandwidth applications with high switching frequencies; iii) Can be combined with using an even number of levels or other balanc-

ing approaches to provide good balancing in all cases; iv) Acceleration of the dynamic voltage balancing and transient response by reducing transient inductance; v) Inherent ripple reduction that can improve efficiency, switch stress, and saturation flux requirements, all with a smaller size than multiple discrete inductors.

We now summarize general design guidelines for robust flying capacitor voltage balancing using coupled inductors. Ripple reduction is a primary function of coupled inductor and multilevel converter design. The design guidelines for this purpose have been explored in detail [12, 22, 26–28, 68, 69]. In general, the ripple can be reduced by interleaving, increasing the number of phases, increasing the number of levels, and designing tightly coupled inductors.

To minimize capacitor voltage imbalances in FCML converters using coupled inductors, the following guidelines are recommended for selecting the number of phases, flying capacitor levels, and coupling coefficients:

1. **Use an even number of phases**: coupled inductor balancing works for an even number of phases and is not effective for an odd number of phases.

2. **Avoid using very high number of phases**: the balancing mechanism gets weaker as the number of phases increases.

3. **Use an even number of levels**: while coupled inductor balancing works for any finite number of levels, an even number of levels aids capacitor voltage balancing in coupled and uncoupled FCML converters alike, especially at nominal conversion ratios.

4. **Maximize the coupling coefficient**: maximizing the coupling coefficient minimizes the imbalance and offers the most ripple reduction for a given transient response.

2.8 Chapter Summary

This chapter proves that coupled inductors are effective at balancing flying capacitor voltages in multiphase FCML converters. The voltage balancing capabilities are derived for an arbitrary multiphase converter, and it is shown that any even number of phases may be balanced for most

duty cycles, and the magnitude of the steady-state imbalances may be predicted theoretically. Multiphase converters with more than two phases are shown to have singularities at certain duty cycles where balancing fails, though these may be suppressed in practical designs. With other conditions held constant, two-phase coupled inductors are shown to minimize the imbalance without susceptibility to singularities that higher-order coupled inductors have. Coupled inductors are shown to balance FCML converters with any number of levels if the coupling ratio is high enough, and may be used to balance any number of flying capacitors so long as there are an even number of phases. Partially coupled inductors will also balance the flying capacitors in some cases, though some coupling ratios will result in divergence. Coupled inductor balancing is shown to apply to a variety of disturbances and to intrinsically unbalanced FCML structures. The theoretical results are experimentally verified with a four-phase, three-level FCML converter, a four-phase, four-level FCML converter, and a two-phase, five-level FCML converter. Design guidelines for the number of phases, number of levels, and coupling coefficient for robust FCML converters are recommended.

3

Demystifying the Multi-Resonant Dynamics of Scalable Power Architectures

The contents of this chapter were previously published under D. H. Zhou and M. Chen, IEEE Transactions on Power Electronics, 2025.

Abstract

This chapter investigates dynamic balancing of flying capacitor multilevel (FCML) converters with coupled inductors. Coupled inductors help to reduce the ripple current, accelerate transient response, and balance the flying capacitors of FCML converters at steady-state. However, coupled inductors also change the dynamic balancing properties compared to uncoupled inductors, and these principles must be understood for robust design. As an extension of a previously developed feedback mechanism for understanding the steady-state behaviors of coupled inductors in FCML converters, this chapter derives models of coupled inductor FCML converters in dynamic operation, revealing several key insights: (i) the multi-resonant behavior of large-order FCML converters and their dependence on the initial conditions, (ii) how power dissipation relates to balancing speed, and (iii) the relation between multiphase and multi-level FCML balancing. The insights uncovered by this chapter can provide useful guidelines for designing multi-phase self-balanced FCML converters with coupled inductors.

3.1 Chapter Introduction

Flying capacitor multilevel (FCML) converters [30] are an important class of converters that leverage interleaved switching devices to generate multiple switching levels, reducing current ripple and transient response time in sensitive applications such as CPU voltage regulators [24, 47], envelope trackers, and power amplifiers [13, 48], especially as the power level increases [12, 42, 49–51]. Compared to traditional buck converters, FCML converters benefit from replacing inductor volume with more energy-dense flying capacitors and switches with lower blocking voltages [25].

However, the advantages of FCML converters are predicated on the flying capacitor voltages being at their balanced levels. If they are not balanced, the switching levels will be corrupted, which increases output distortion, switch stress, and current ripple [34–37]. In practice, this limitation has posed a major barrier to the adoption of FCML converters despite their theoretical

benefits [38]. As a result, considerable effort has been made to investigate how FCML converters become unbalanced and what mechanisms can be used to balance them. FCML balancing is complicated by the fact that it is a fundamentally higher-order effect, as established in seminal early works such as [34–36], thus precluding the use of standard state-space averaging methods. This first generation of work used frequency domain decomposition of the switching waveforms to establish the existence of natural balancing, a property possessed by practical FCML converters that have parasitic losses. Natural balancing essentially refers to the process where flying capacitor imbalances dissipate themselves by the losses they cause in the switches, load, or output network.

These results, while thorough, were relatively complex, and the second generation of FCML balancing analyses attempted to rectify this by using time-domain methods based on "stitching" piece-wise linear circuit solutions for every switching state of the converter during a full period [43, 62, 63]. These methods produce results consistent with previous frequency domain analysis and emphasized the importance of the PWM (pulse-width modulation) switching scheme to the balancing behavior, thus suggesting the possibility of improving balancing by optimal sequencing of redundant switch states [43]. Two drawbacks of the time-domain "stitching" methods are their relative informality and the high computational cost.

The current generation of balancing research has built upon, formalized, and refined prior results [32, 38, 44–46, 58, 59, 61, 70]. These works and others improve the state-space models of FCML balancing, in addition to proving how balancing loses robustness or fails at nominal conversion ratios and with converters with an odd number of levels [32, 46]. Many practical aspects of FCML balancing, such as the impact of switch parasitics, high-speed operation [12, 71] and start-up/shut-down dynamics [53] have also been investigated. Because of these developments, FCML balancing analysis now includes the dynamic (what happens when the flying capacitors are not balanced and evolve towards equilibrium) and steady-state (the imbalance that exists even at equilibrium due to some persistent disturbance) [32, 38, 59, 72]. FCML balancing also spans passive, natural, and dissipative methods, along with active balancing where flying capaci-

tor voltages are measured or estimated and actively balanced [39, 40].

Coupled inductors are an effective tool for balancing FCML converters with many levels and many phases by generating circulating currents at steady-state which compensate for disturbances [66, 72], while also improving the ripple and transient properties of the converter [26–28]. However, coupled inductors also affect the balancing dynamics, and it is not fully understood how this changes the converter's behavior during important conditions such as start-up, shut-down, and high-speed operation [71]. Here, we develop two analytical frameworks to explain the dynamics of coupled inductor FCML balancing: first, a model based on power dissipation that produces closed-form solutions for simple converters, and second, a state-space model that captures the multi-resonant balancing dynamics of coupled inductor FCML converters. This work makes several contributions to FCML balancing dynamics, both with and without coupled inductors, by investigating:

- How balancing dynamics can be explained through the loss-context and by tracking the average power being dissipated because of the imbalance.
- The similarity of balancing dynamics for a multiphase and multilevel FCML converter.
- How the initial condition of an unbalanced converter can dramatically affect the balancing dynamics and speed.

The rest of this chapter is organized as follows: section 3.2 reviews the fundamentals of coupled inductor FCML converters. Section 3.3 develops a power dissipation model of simple FCML converters. Section 3.4 extends state-space models of FCML converter balancing to coupled inductors. Finally, the results are experimentally verified in section 3.5 and concluded in section 3.6.

3.2 Operation Principles of the Coupled Inductor FCML Converter

A two-phase, three-level FCML converter with coupled inductors is shown in Fig. 3.1. The two FCML phases each have two pairs of complementary switches and one flying capacitor with an

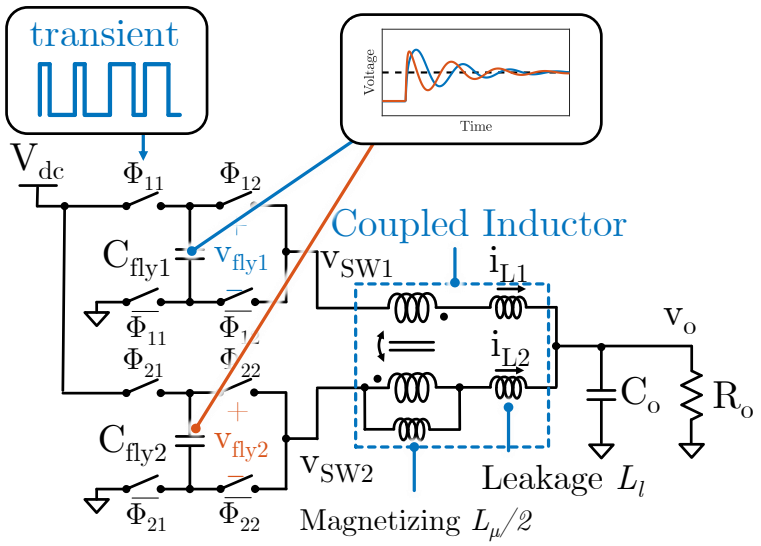


Figure 3.1: Schematic of two-phase, three-level FCML converter with coupled inductors. After a transient unbalances the flying capacitors, they balance back to equilibrium due to losses in the circuit.

ideal balanced voltage of half the input voltage. The switches in one phase are operated with a 180° phase shift such that two evenly spaced pulses are produced at the switch nodes, as shown in Fig. 3.2. The two FCML converters are themselves 90° phase shifted from each other, thus producing four evenly spaced pulses that minimize ripple. This operational scheme is known as phase-shifted pulse width modulation (PS-PWM).

The inductors in Fig. 3.1 are coupled, meaning the windings share a single core as illustrated in Fig. 2.3(b). By sharing the magnetic flux paths between the two phases, the voltage applied to one coil will affect the current in the other. This effect is leveraged to present a low inductance during common-mode transient events and a high inductance to steady-state ripple current [5, 26]. These inductances are represented by the leakage (L_l) and magnetizing (L_μ) inductances of the coupled inductor. As the inductors are more tightly coupled, the magnetizing inductance increases. As the leakage inductance decreases, the transient response is accelerated. However, it is important to switch all phases with equal phase shift when using tightly coupled inductors, as failure to do so will present a very low inductance to some phases at steady-state. In this work, we assume the inductors are fully coupled, meaning the magnetizing inductance is infinite and, as shown in the schematic in Fig. 2.3(a), the currents in both phases of the coupled inductor are

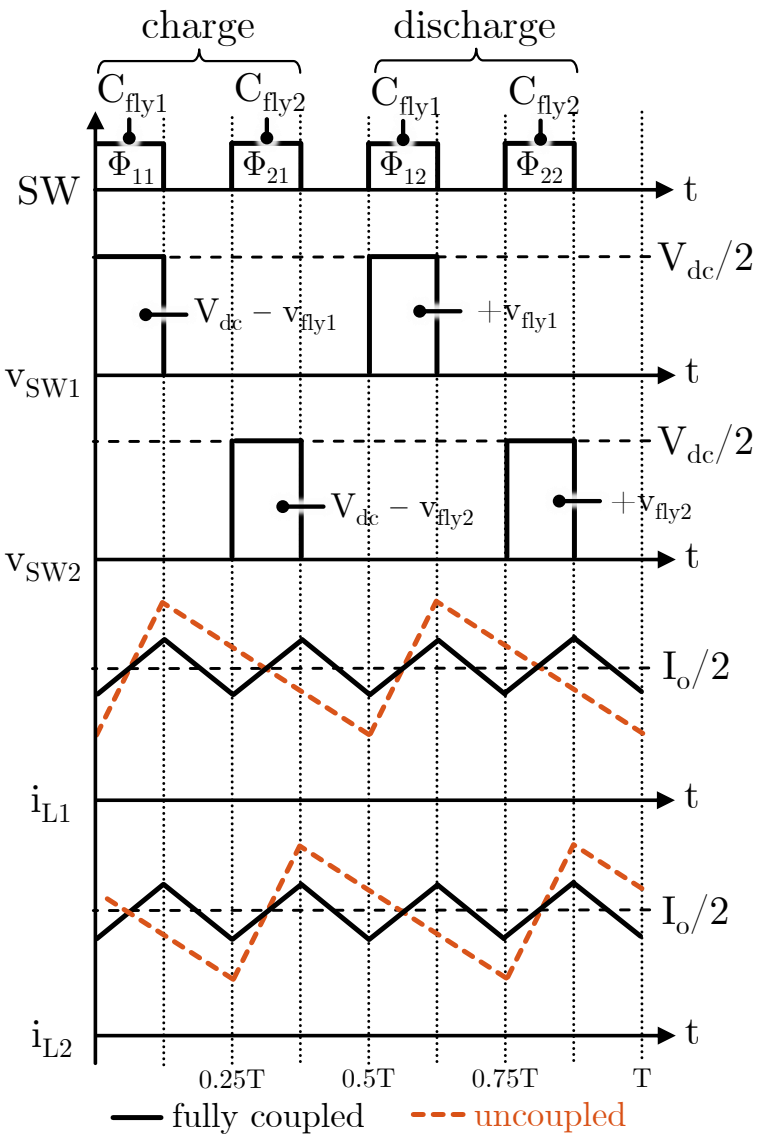


Figure 3.2: Switching waveforms of the two-phase, three-level FCML converter in Fig. 3.1 with PS-PWM and $d = 0.125$. If the inductors are fully coupled, the per-phase currents are equal both in average and in ripple.

equal to

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{v_{L1} + v_{L2}}{2L_l}. \tag{3.1}$$

This is also shown in the waveforms in Fig. 3.2.

To analyze the balancing behavior of coupled inductors in FCML converters with multiple phases and levels, we define the number of phases as M and the number of flying capacitors as K, meaning each phase is a $(K+2)$-level FCML converter since each flying capacitor adds one more switching voltage level in addition to GND and V_{dc}. We denote the flying capacitor voltages as $v_{\mathrm{fly}}^{(\text{phase \#m, cap \#k})}$, or for brevity, $v_{\mathrm{fly}}^{(\mathrm{m,k})}$, where $m = 1, \ldots, M$ and $k = 1, \ldots, K$ are the indices identifying the phase and capacitor. The capacitor closest to the input source has the index $k = 1$.

In developing the two models, we make frequent use of the small-signal imbalance voltages and currents of the FCML converter [72]. This allows us to focus on the balancing behavior of interest. In this work, we use tildes to denote small-signal imbalance components of interest. For an M-phase, $(K+2)$-level converter, there are $M \times K$ total flying capacitors with voltages

$$v_{\mathrm{fly}}^{(m,k)} = v_{\text{fly, balanced}}^{(m,k)} + \tilde{v}_{\mathrm{fly}}^{(m,k)}, \tag{3.2}$$

split into balanced and unbalanced components. The ideally balanced voltage of each flying capacitor is

$$v_{\text{fly, balanced}}^{(\mathrm{m,\,k})} = V_{\mathrm{dc}} \frac{K+1-k}{K+1}, \tag{3.3}$$

which is the voltage that they return to under the influence of natural balancing. External disturbances such as input impedances, transient events, or timing mismatches can cause the flying capacitor voltages to leave equilibrium [38, 72]. More detailed analyses of FCML converter operation can be found in works such as [30, 35, 72], and more detailed models of coupled inductors can be found in [26].

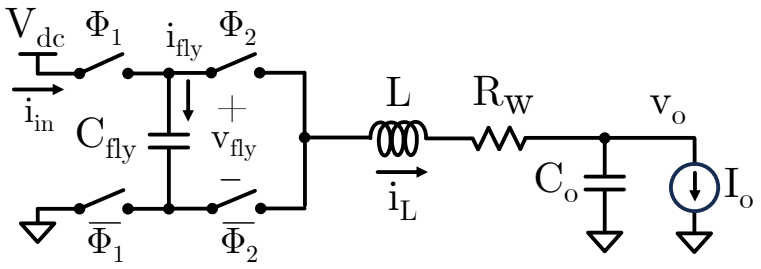


Figure 3.3: Schematic of a three-level FCML converter.

3.3 Internal Dynamics of Simple Multilevel Converters Explained via Power Dissipation

3.3.1 Motivation

By studying FCML dynamics, we wish to understand how the converter transitions from an unbalanced initial condition to a balanced equilibrium, and what factors affect the speed and stability of said transition. As introduced in section 3.1, natural balancing occurs in FCML converters because imbalanced flying capacitors cause additional losses in the converter that balance the system over time. Many factors such as the switching frequency and inductor quality factor affect the magnitude of loss and thus the balancing speed; we term these factors the "loss-context" of the converter. While the qualitative impact of these factors have been understood from early studies [30, 34, 57] onward, their quantitative relation to balancing is less clear since most current dynamic models are not derived from the root cause of balancing, which is power dissipation.

In this section, we model FCML balancing dynamics by directly calculating the power dissipation caused by unbalancing and the balancing dynamics that result. Using this method, we reveal the direct analytical link between the loss-context and balancing speed of simple one- and two-phase three-level FCML converters, adding depth and support to existing research results.

3.3.2 Assumptions

The analytical methods are tenable only with several important simplifying assumptions. They are enumerated here, along with the importance and justification of each.

Table 3.1: PLECS Simulation of Balancing Time [ms] vs. Large-Signal Input/Output Conditions

	V_{dc} [V]			
I_o [A]	4	8	12	16
0	120.0	120.0	120.2	120.2
5	121.5	121.6	121.7	121.8
10	123.0	123.1	123.2	123.2
15	124.5	124.6	124.6	124.7

1. The flying capacitors C_{fly} are large enough such that the flying capacitor voltages are approximately constant in one period. This simplifies the period-by-period discretization of the dynamics and is valid because practical converters need small flying capacitor voltage ripple to maintain a stable switch node voltage level and to protect the switches from overvoltage. The output capacitance is assumed to be large enough such that the output voltage is approximately constant.

2. The quality factor of the inductor is high and the current ramps up and down approximately linearly. This simplifies the current and loss calculations and is valid because practical converters usually have high inductor quality factor for high efficiency.

3. The loss is represented by a winding resistor R_w. The analysis is limited to loss sources that can be reasonably represented in this way and is not applicable to, for example, nonlinear loss sources.

4. When analyzing coupled inductor converters, they are assumed to be fully coupled. This simplifies the equivalent circuits and current calculations. A justification is provided in section 3.4.3.

3.3.3 Model Derivation

Our derivation stems from the observation that three-level converters generally balance exponentially with a time constant that does not depend on the input voltage level or output current, as exemplified by the PLECS simulation results in Table 3.1 for a simple three-level converter

(Fig. 3.3) with $f_{\text{sw}} = 500$ kHz, $d = 0.25$, $C_{\text{fly}} = 50$ μF, $L = 1$ μH, $R_w = 10$ mΩ, $C_o = 100$ μF, and an initial 2 V imbalance. The apparent independence of balancing speed from large signal conditions suggest that the power dissipation causing balancing is dependent only on the imbalance magnitude. To investigate this, we begin by noting the inductor current can be split into three components shown in Fig. 3.4: the load current I_o, a ripple component i_{ripple}, and the current induced by the unbalanced flying capacitors $\tilde{i}_L$, the latter of which is only possessed by the unbalanced system. The average value of the ripple and imbalance component are both assumed to be zero. The instantaneous loss in the resistor R_w is therefore

$$P_{R_w}(t) = R_w i_L(t)^2 = R_w \left[I_o + i_{\text{ripple}}(t) + \tilde{i}_L(t) \right]^2 . \tag{3.4}$$

The instantaneous power dissipation changes with time and is evidently dependent on the large signal conditions. To simplify the analysis, we discretize the continuous balancing system into steps of duration T. We do this by assuming the flying capacitor voltage is constant over the period T (large C_{fly}), then update it at the end of every period using the average power dissipation over the period. This discretization is valid since the capacitor balancing dynamics in practical converters with large C_{fly} and small losses are much slower than the period. The average power dissipation in the resistor over a period is

$$\overline{P_{R_w}}(t) = R_w \left\langle i_L(t)^2 \right\rangle , \tag{3.5}$$

where $\langle x(t) \rangle = \frac{1}{T} \int_t^{t+T} x(\zeta) \, \mathrm{d}\zeta$ is the average of a function over one period. We expand and simplify eq. (3.5) to find

$$\begin{aligned} \overline{P_{R_w}}(t) &= R_w \left\langle \left[I_o + i_{\text{ripple}}(t) + \tilde{i}_L(t) \right]^2 \right\rangle \\ &= R_w I_o^2 + R_w \left\langle i_{\text{ripple}}(t)^2 \right\rangle + R_w \left\langle \tilde{i}_L(t)^2 \right\rangle \\ &\quad + 2R_w I_o \left\langle i_{\text{ripple}}(t) \right\rangle + 2R_w I_o \left\langle \tilde{i}_{\text{L}}(t) \right\rangle \\ &\quad + 2R_w \left\langle i_{\text{ripple}}(t) \tilde{i}_{\text{L}}(t) \right\rangle . \end{aligned} \tag{3.6}$$

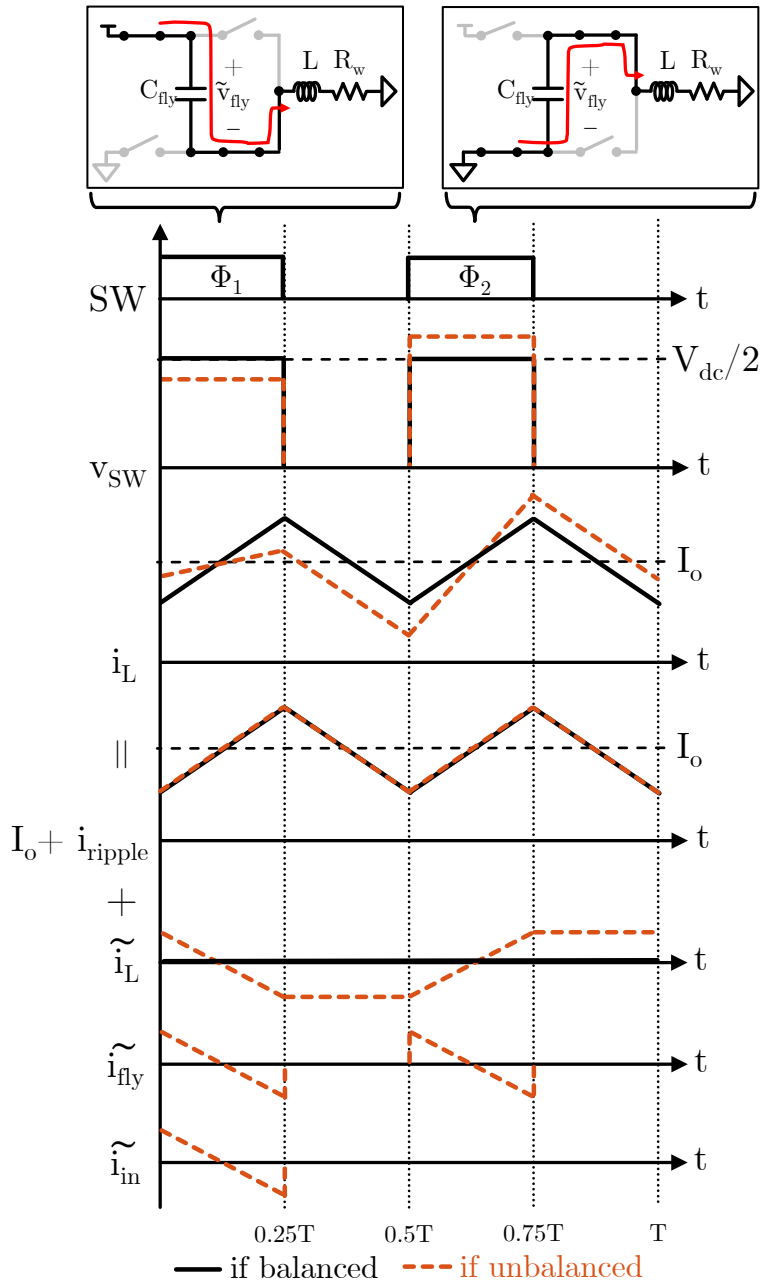


Figure 3.4: Large- and small-signal components of the inductor current ripple in a balanced and unbalanced FCML converter.

Eq. (3.6) can be simplified by noting the average of the ripple and imbalance components over a period are zero. Furthermore, $\left\langle i_{\text{ripple}}(t)\tilde{i}_{\text{L}}(t)\right\rangle = 0$ since the two functions are orthogonal when averaged over a period. This can be inspected in Fig. 3.4; both functions have zero average, are symmetric, but the ripple current has twice the frequency. Therefore, the average power dissipation is

$$\overline{P_{R_w}}(t) = R_w I_o^2 + R_w \left\langle i_{\text{ripple}}(t)^2\right\rangle + R_w \left\langle \tilde{i}_L(t)^2\right\rangle . \tag{3.7}$$

The difference between the average power dissipation in a balanced $\left(\tilde{i}_L = 0\right)$ and unbalanced $\left(\tilde{i}_L \neq 0\right)$ converter is $R_w \left\langle \tilde{i}_L(t)^2\right\rangle$, which depends only on the imbalanced components and not on the steady-state load or ripple. In addition to the power dissipated in R_w, we see by inspection of Fig. 3.3, there are two more power sinks (the load and charging C_{fly}) and one power source (V_{dc}) in the converter. During each period, the power sources and sinks must cancel to

$$\overline{P_{\text{in}}}(t) - \overline{P_{R_w}}(t) - \overline{P_{\text{fly}}}(t) - \overline{P_{\text{o}}}(t) = 0. \tag{3.8}$$

Here, the average output power is

$$\overline{P_{\text{o}}}(t) = \langle I_o(dV_{\text{dc}} - i_L(t)R_w)\rangle = dV_{\text{dc}}I_o - R_w I_o^2, \tag{3.9}$$

and the average input power is

$$\overline{P_{\text{in}}}(t) = \langle V_{\text{dc}} i_{\text{in}}(t)\rangle = V_{\text{dc}} \left(dI_o + \left\langle i_{\text{ripple}}(t) + \tilde{i}_L(t)\right\rangle_t^{t+dT}\right), \tag{3.10}$$

where $\langle x(t)\rangle_a^b = \frac{1}{T}\int_a^b x(t)\,\mathrm{d}t$. The average power into the flying capacitor, following from Fig. 3.4, is

$$\begin{aligned}\overline{P_{\text{fly}}}(t) &= \langle v_{\text{fly}}(t) i_{\text{fly}}(t) \rangle \\ &= v_{\text{fly}}(t) \left(\langle i_L(t) \rangle_t^{t+dT} - \langle i_L(t) \rangle_{0.5T}^{(0.5+d)T} \right) \\ &= v_{\text{fly}}(t) \left(2 \left\langle \tilde{i}_L(t) \right\rangle_t^{t+dT} \right), \end{aligned} \tag{3.11}$$

where $v_{\text{fly}}(t) = \frac{V_{\text{dc}}}{2} + \tilde{v}_{\text{fly}}(t)$. Since the flying capacitor sees the inductor current twice per period in opposite directions and equal durations, the ripple and load component cancel out in average. Only the imbalance component causes any average power transfer to the flying capacitor. Substituting eqs. (3.7), (3.9), (3.10), and (3.11) into eq. (3.8) yields

$$\begin{aligned} &V_{\text{dc}} \left\langle i_{\text{ripple}} \right\rangle_t^{t+dT} - R_w \left\langle i_{\text{ripple}}(t)^2 \right\rangle \\ &- 2\tilde{v}_{\text{fly}} \left\langle \tilde{i}_L(t) \right\rangle_t^{t+dT} - R_w \left\langle \tilde{i}_L(t)^2 \right\rangle = 0 \end{aligned} \tag{3.12}$$

after canceling most terms. Eq. 3.12 must be satisfied for all values of the imbalance, even when the converter is balanced and $\tilde{i}_L(t) = 0$. This implies that

$$V_{\text{dc}} \left\langle i_{\text{ripple}} \right\rangle_t^{t+dT} = R_w \left\langle i_{\text{ripple}}(t)^2 \right\rangle, \tag{3.13}$$

because the dissipation caused by the ripple current in R_w must be compensated by more power coming from the input. If we then substitute eq. (3.12) and (3.13) into eq. (3.11), we conclude that the average power into the flying capacitor is

$$\overline{P_{\text{fly}}}(t) = -v_{\text{fly}}(t) \times \frac{R_w \left\langle \tilde{i}_L(t)^2 \right\rangle}{\tilde{v}_{\text{fly}}(t)} \tag{3.14}$$

We now calculate the difference in average power dissipation between a balanced and unbalanced converter

$$\begin{aligned} R_w \left\langle \tilde{i}_L(t)^2 \right\rangle &= \frac{R_w}{T} \int_0^T \tilde{i}_L(t)^2 \mathrm{d}t \\ &= \frac{R_w T^2 d^2 (3 - 4d) \tilde{v}_{\text{fly}}(t)^2}{12 L^2} = \frac{\tilde{v}_{\text{fly}}(t)^2}{R_{\text{eff}}}, \end{aligned} \tag{3.15}$$

for $d \leq 0.5$ (mirrored for $d > 0.5$), with details in Appendix B.1. $R_{\text{eff}} = \frac{12L^2}{R_w T^2 d^2 (3-4d)}$ is the effective resistance that takes into account all relevant loss-context factors: the series resistance R_w, switching frequency, duty cycle, and inductance. A final substitution into (3.14) yields

$$\overline{P_{\text{fly}}}(t) = -\frac{v_{\text{fly}}(t) \times \tilde{v}_{\text{fly}}(t)}{R_{\text{eff}}}, \tag{3.16}$$

the average power into the flying capacitor, which depends on both the balanced and unbalanced components of the flying capacitor voltage. Having found the average power into the flying capacitor, we now consider energy stored in it,

$$E_{\text{fly}}(t) = \frac{1}{2} C_{\text{fly}} v_{\text{fly}}(t)^2. \tag{3.17}$$

The change in energy in flying capacitor energy between periods is

$$\Delta_T[E_{\text{fly}}(t)] = \overline{P_{\text{fly}}}(t) \times T, \tag{3.18}$$

where $\Delta_T[E_{\text{fly}}(t)] = E_{\text{fly}}(t+T) - E_{\text{fly}}(t)$ denotes the forward difference of a function. Expanding (3.18) with eqs. (3.17) and (3.16) yields

$$\begin{aligned}
\frac{1}{2} C_{\text{fly}} \Delta_T[v_{\text{fly}}(t)^2] &= -\frac{v_{\text{fly}}(t) \times \tilde{v}_{\text{fly}}(t)}{R_{\text{eff}}} \times T \\
\frac{V_{\text{dc}} \Delta_T[\tilde{v}_{\text{fly}}(t)]}{T} + \frac{\Delta_T[\tilde{v}_{\text{fly}}(t)^2]}{T} &= -\frac{2 v_{\text{fly}}(t) \times \tilde{v}_{\text{fly}}(t)}{C_{\text{fly}} R_{\text{eff}}} \\
V_{\text{dc}} \frac{\mathrm{d}\tilde{v}_{\text{fly}}(t)}{\mathrm{d}t} + \frac{\mathrm{d}\tilde{v}_{\text{fly}}(t)^2}{\mathrm{d}t} &\approx -V_{\text{dc}} \frac{\tilde{v}_{\text{fly}}(t)}{C_{\text{fly}} R_{\text{eff}}} - 2 \frac{\tilde{v}_{\text{fly}}(t)^2}{C_{\text{fly}} R_{\text{eff}}}
\end{aligned} \tag{3.19}$$

Here, we apply the forward approximation of the derivative $\frac{\Delta_T[x(t)]}{T} \approx \frac{\mathrm{d}x(t)}{\mathrm{d}t}$. The solution for the flying capacitor imbalance voltage that satisfies (3.19) is

$$\tilde{v}_{\text{fly}}(t) = \tilde{v}_{\text{fly}}(0) e^{-\frac{t}{C_{\text{fly}} R_{\text{eff}}}}, \tag{3.20}$$

Eq. (3.20) implies that the imbalance voltage decays exponentially, matching existing literature,

with time constant $\tau_{M=1} = C_{\text{fly}} R_{\text{eff}} = \frac{12 C_{\text{fly}} L^2}{R_w T^2 d^2 (3-4d)}$. The dependence on the loss-context is clear. The balancing time is faster with smaller flying capacitors or high loss, through low quality factor, lower switching frequency (leading to higher peak currents), or with higher duty cycle (such that the flying capacitors are connected to the output for a longer part of the period.) If we substitute the parameters used for the simulations in Table 3.1, eq. (3.20) predicts a balancing time of 120 ms.

The PLECS simulation results in Fig, 3.5 verify the mathematical derivations with $V_{\text{dc}} = 16$ V, $I_o = 5$ A, and the same component parameters as before. Two parallel simulations are performed, one with a balanced flying capacitor, and one with a 2 V starting imbalance. This generates balanced and unbalanced flying capacitor voltages ($v_{\text{fly,u}}(t)$, $v_{\text{fly,b}}(t)$) and inductor currents ($i_{L,u}(t)$, $i_{L,b}(t)$), the unbalanced versions of which are plotted. The third plot verifies the average power formulations of equations (7) and (15). The fourth plot verifies both sides of the energy step equation (18).

3.3.4 Comparison to Coupled Inductors

The power dissipation method also applies to the two-phase, three-level coupled FCML converter illustrated in Fig. 3.1 applying the same assumptions as before. For the two-phase converter, there are two flying capacitors causing an average power loss

$$R_w \left\langle \tilde{i}_L(t)^2 \right\rangle = \frac{R_w T^2 d^2 (3-4d) \|\tilde{\mathbf{v}}_{\text{fly}}\|^2}{24 L_l^2} = \frac{\|\tilde{\mathbf{v}}_{\text{fly}}\|^2}{R_{\text{eff}}}, \tag{3.21}$$

where $\tilde{\mathbf{v}}_{\text{fly}}$ is a vector of the imbalance voltages and $\|.\|$ is the Euclidean norm. The average power loss over a period only depends on the normalized imbalance voltage $\|\tilde{\mathbf{v}}_{\text{fly}}\|$. This is important since it enables us to solve an power-balance equation by treating $\|\tilde{\mathbf{v}}_{\text{fly}}\|^2$ as the dynamic variable:

$$\|\tilde{\mathbf{v}}_{\text{fly}}(t)\| = \|\tilde{\mathbf{v}}_{\text{fly}}(0)\| e^{-\frac{t}{C_{\text{fly}} R_{\text{eff}}}} \tag{3.22}$$

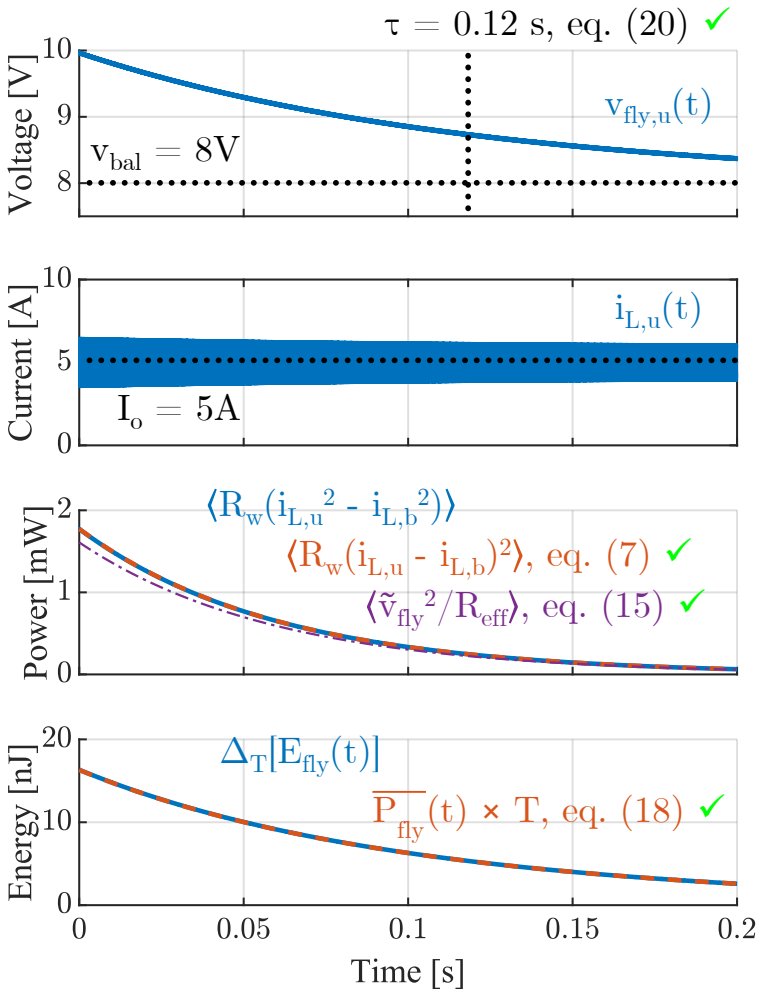


Figure 3.5: PLECS simulation verification of key equations in derivation of the power dissipation model of balancing.

The normalized imbalance of the two-phase converter therefore decays with time constant

$$\tau_{M=2} = \frac{24 C_{\text{fly}} L_l^2}{R_w T^2 d^2 (3 - 4d)}, \tag{3.23}$$

which is identical to the one-phase case except depending on the leakage inductance L_l and with a different scaling factor. The fundamental natural balancing mechanism acting on the circuits is the same. The leakage inductance can be designed to be much smaller than the discrete inductance of an uncoupled converter due to the ripple reduction and cancellation effect of interleaving and coupling [26]. The maximum ripple across the duty cycle range of a coupled and uncoupled converter will be the same if the leakage inductance is designed to be $L_l = \frac{L}{M^2}$ [73]. In this case,

the ratio between the balancing times is

$$\frac{\tau_{\mathrm{M=2}}}{\tau_{\mathrm{M=1}}} = \frac{1}{8}. \tag{3.24}$$

A two-phase coupled inductor converter can balance eight times faster than an uncoupled converter without changing the ripple. Even if the leakage inductance is not minimized, it can still accelerate the dynamics of a coupled converter significantly.

By solving for the power dissipation directly, this model reveals the fundamental mechanism of natural balancing. Our results confirm those in previous literature [34] and emphasize the importance of loss on the dynamics: more generally than just the actual loss source (winding resistance, core loss, switching loss, etc.), the dynamics depend on the loss-context. If the condition is lossy, such as a low switching frequency that generates high peak square currents, the dynamics will be faster.

The limitation of the power dissipation model is that it cannot be used for more complex coupled FCML converters. While they still have the same fundamental balancing mechanism, we cannot generally express the loss as a function of the normalized imbalance only, and thus cannot write a differential equation like in eq. (3.22). This is because there are generally multiple dynamic modes for more complex converters and the balancing dynamics depend not only on the normalized imbalance, but also on the individual voltages. To explore this phenomenon, we develop a dynamic model based on formal state-space analysis for coupled inductor FCML converters in the next section.

3.4 Multi-Resonant Dynamics of Multiphase FCML Converters

To address the shortcomings of the power dissipation model, we develop a more general state-space dynamic model in this section. Many prior works have developed comprehensive state-space models for the balancing dynamics of FCML converters with a single phase [40, 46, 58], which we we extend coupled inductor FCML converters. Since the mathematical modifications from uncoupled FCML models in previous works are minor, the details are contained in Ap-

pendix B.2. The steps to derive a generalized dynamic model of an FCML converter typically consists of (i) describing the switching states, (ii) reducing the circuit to an equivalent circuit at each switching state, (iii) solving the equivalent circuit for each sub-period, (iv) combining the sub-period solutions, and (v) analyzing the dynamics of the combined solution.

In developing this model, we reveal the multi-resonant dynamic behavior of larger-order coupled FCML converters ($M \geq 4$), where there exist multiple balancing modes of drastically different speed that are excited depending on the initial conditions of the imbalance.

3.4.1 State-Space Model for Coupled Inductor FCML Balancing Dynamics

The main adaptation required from previous models is the reduction of the coupled inductor circuit. As before, we assume fully coupled inductors. Fig. 3.6 shows the reduction of the full circuit schematic for a given switching state. For a generalized M-phase, $(K+2)$-level converter, there will be a total of $2M(K+1)$ switching states, during each of which a set of flying capacitors are connected to the output (example shown in (a)). (b) reduces the circuit to its small-signal imbalance components. Because of the coupled inductor, we must add step (c), where fully coupled inductors are assumed; therefore, the current in each phase is equal, and the multiphase circuit is equivalent to placing all the capacitors in series since they all charge/discharge with the same current. Finally, the circuit is reduced to (d) with one equivalent capacitance. Of interest is the fact that if the inductors are fully coupled, adding more phases has a very similar effect to adding more levels on the balancing dynamics. The equivalent circuit is still a sum of capacitors connected in series.

The equivalent circuit in Fig. 3.6(d) is solved for each of the switching sub-periods, then each sub-period solution is combined to produce a discrete state transition matrix that updates the state variables through a switching period

$$\tilde{\mathbf{x}}(T) = \mathbf{T}_{\text{full}}\tilde{\mathbf{x}}(0), \tag{3.25}$$

which we then convert using the forward approximation of the derivative to derive a continuous

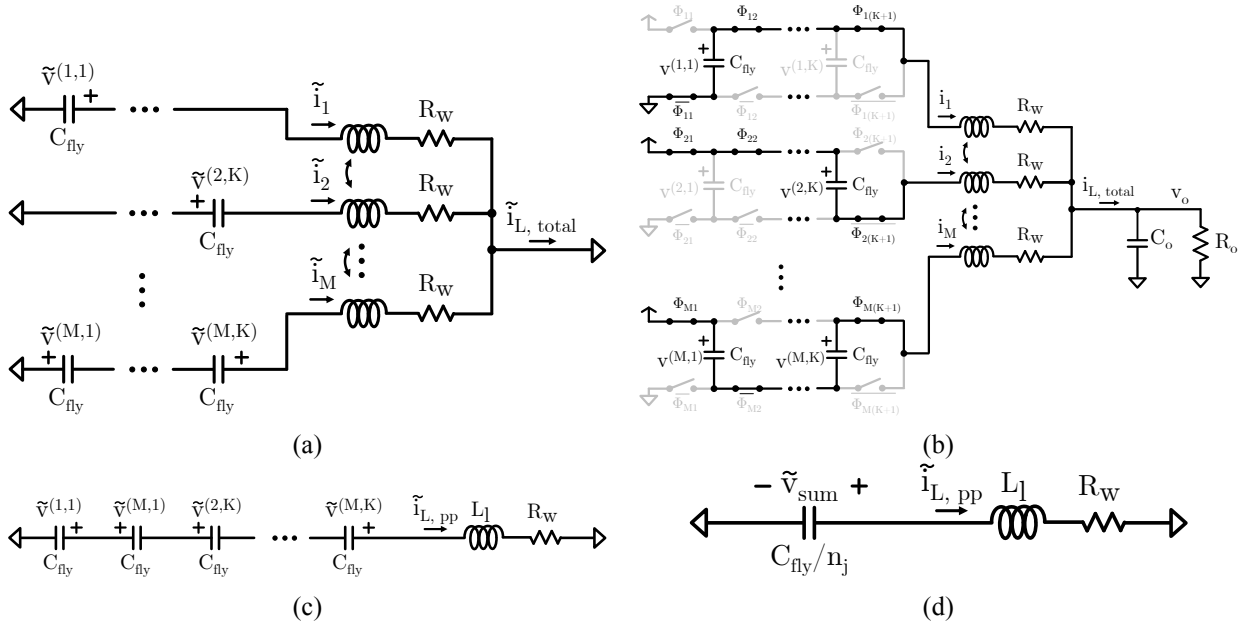


Figure 3.6: (a) Full schematic for a given switching state, before reduction. (b) Schematic with only small-signal imbalances. (c) Coupled inductor reduction into one equivalent phase. (d) Final reduced schematic with only one equivalent capacitance, inductance, and resistance.

model

$$\frac{\mathrm{d}\tilde{\mathbf{x}}(t)}{\mathrm{d}t} \approx \mathbf{A}\tilde{\mathbf{x}}(t), \tag{3.26}$$

where

$$\tilde{\mathbf{x}} = \begin{bmatrix} \tilde{v}_{\text{fly}}^{(1,1)} & \cdots & \tilde{v}_{\text{fly}}^{(1,K)} & \tilde{v}_{\text{fly}}^{(2,1)} & \cdots & \tilde{v}_{\text{fly}}^{(M,K)} & \tilde{i}_L \end{bmatrix}^{\mathrm{T}} \tag{3.27}$$

is a vector of the state variables. The details of this derivation are contained in Appendix B.2. The internal state-space matrix $\mathbf{A}$ reveals the dynamics of FCML converter balancing. Through eigenanalysis, we can find the modes of imbalance decay and their relation to the starting imbalance $\tilde{\mathbf{x}}(0)$.

3.4.2 Effect of Initial Condition on FCML Converter Balancing

Like a higher-order single phase FCML converter, coupled inductor FCML converters can form damped resonant circuits when balancing. This happens because the flying capacitors exchange energy through the coupled inductors. We begin with the illustrative simulation of a four-phase,

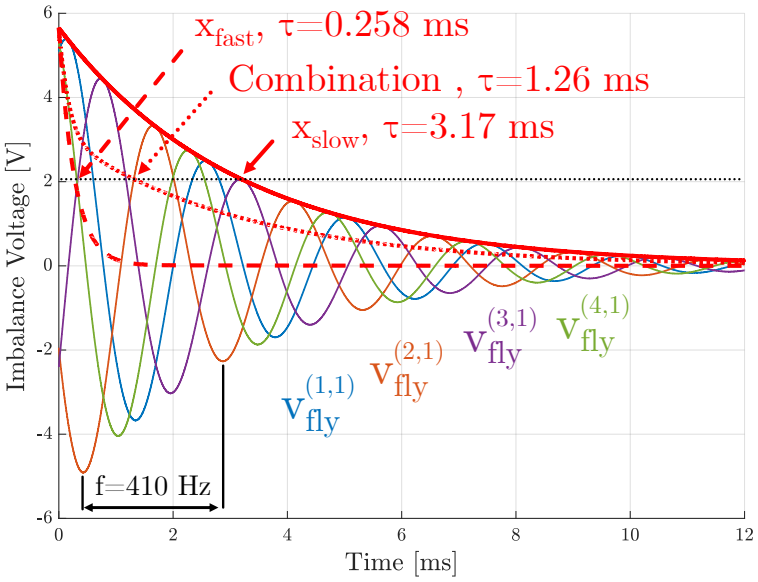


Figure 3.7: Simulation of four-phase, three-level FCML converter balancing from different initial imbalances, demonstrating multi-resonant properties.

Table 3.2: Simulation Parameters of the FCML Converter

f_{sw}	d	V_{dc}	C_{fly}	L_l	L_μ	R_w
500 kHz	0.5	16 V	50 μF	$\frac{1}{M^2}\mu H$	$100\times L_l$	10 mΩ

three-level converter with $f_{sw} = 500$ kHz, $d = 0.125$, $C_{fly} = 50$ μF, $L_l = 62.5$ nH, $C_o = 1$ mF, and $R_w = 50$ mΩ in Fig. 3.7. Eigenanalysis of the state-space matrix $\mathbf{A}$ for this converter reveals the system has three modes: a fast oscillatory mode with frequency 2.23 kHz and time constant 0.281 ms, a slow oscillatory mode with frequency 405 Hz and time constant 3.14 ms, and one quickly decaying R-L mode that is dominated by the other two.

The two oscillatory modes describe the ways the flying capacitor voltages can balance. In particular, the time constants show the time that it takes for the initial imbalance $\|\tilde{\mathbf{v}}_{fly}(0)\|$ to decay to $e^{-1}\times$ its original value. The two time constants are separated by an order of magnitude, which can have a major impact on the transient speed of the converter. The cause of the different balancing times is the initial condition. Depending on what the initial imbalances $\tilde{\mathbf{v}}_{fly}(0)$ are, different modes will be excited, which can result in drastically different balancing times. Thus, a converter with multiple flying capacitors can form a multi-resonant system where the initial condition affects the balancing dynamics.

Table 3.3: Simulated Balancing Time with Common-Mode and Differential-Mode Imbalances

# Phases M	1	2	4	6	8	16
$\tau_{\text{common-mode}}$ [ms]	60.1	7.44	1.53	1.29	0.61	0.061
$\tau_{\text{differential-mode}}$ [ms]	60.1	7.44	30.8	41.3	46.1	52.2

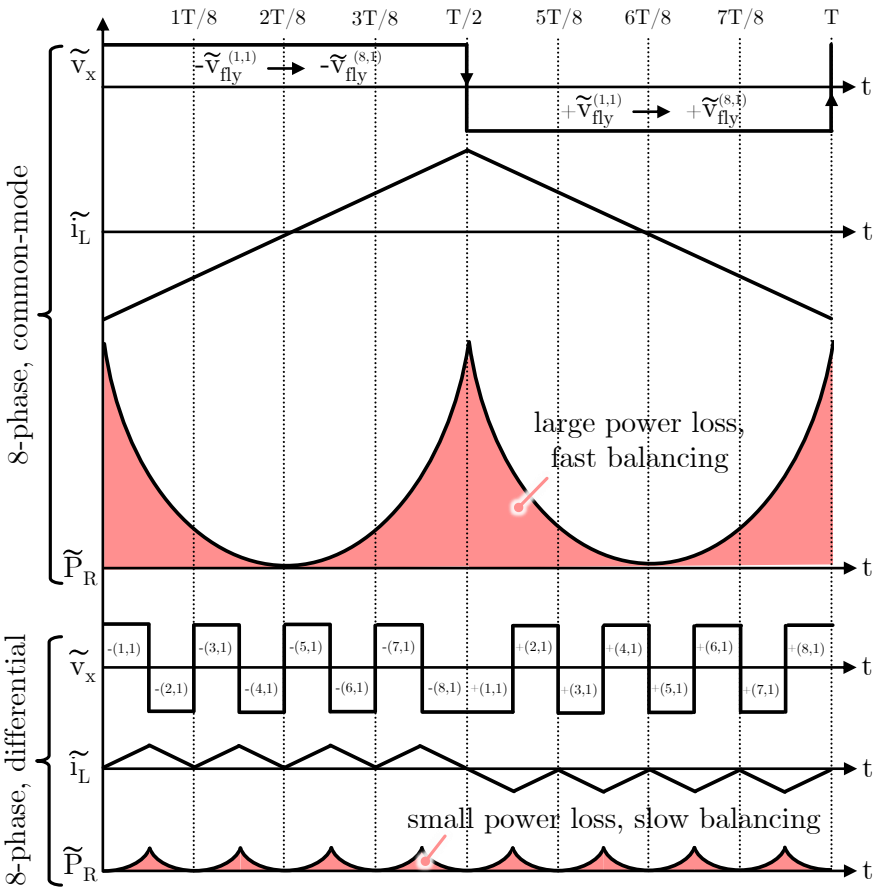


Figure 3.8: Waveforms of an eight-phase converter with $d = \frac{1}{16}$ demonstrating the effect of a fast (common-mode) and slow (differential-mode) initial condition on the amount of imbalance energy dissipated in a period.

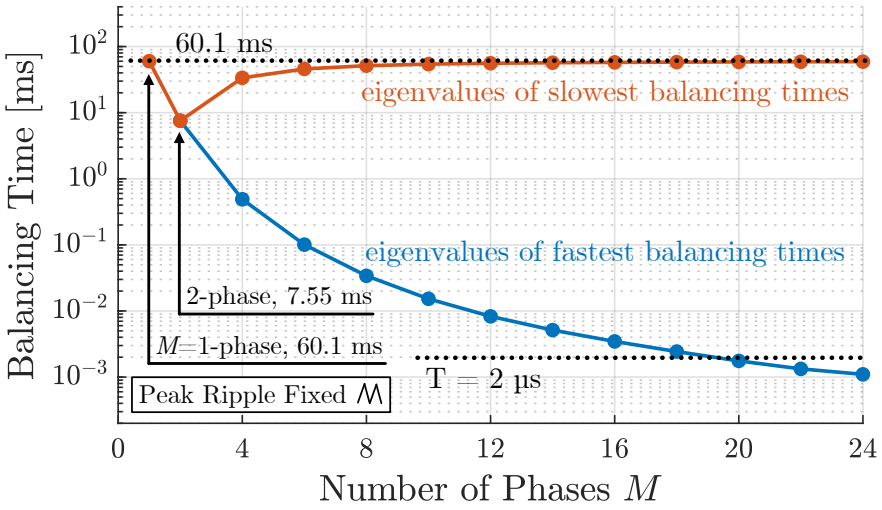


Figure 3.9: Fastest and slowest eigenvalues of the balancing time of multiphase three-level FCML converters with ripple current held constant as the number of phases rises using the inductance parameters in Table 3.2. The model predictions below the switching period $T = 2\ \mu$s are included for completeness, but do invalidate the assumptions in Section 3.3.2

.

Fig. 3.7 verifies the two predicted time constants by setting the four initial imbalances to those associated with the fast and slow modes. In both cases, the envelope of the imbalance $\|\tilde{\mathbf{v}}_{\text{fly}}(t)\|$ decays exponentially with the predicted speed. If the initial condition is a combination of the two, then the decay is a combination of the two modes.

This analysis also reveals why the power dissipation model does not work for more complex FCML converters; a multi-resonant converter has multiple balancing modes. When computing the power dissipation model, we assumed a single exponential balancing mode, which cannot account for conditions where more than one mode is excited.

We consider two common cases for initial imbalances: (i) Common-Mode, where all initial imbalances are equal, such as during start-up or shut-down, and (ii) Differential-Mode, where the initial imbalance voltages are equal in magnitude and alternate in sign, which often results from external disturbances [65]. Using the circuit parameters shown in Table 3.2, which keeps the maximum ripple current equal as the number of phases changes, we simulate the balancing time with a purely common-mode and differential imbalance for converters up to $M = 16$ phases. Except for the two-phase converter, which has only one mode, the common-mode time constant is always much smaller than the differential-mode case. The reason is illustrated in Fig. 3.8 with

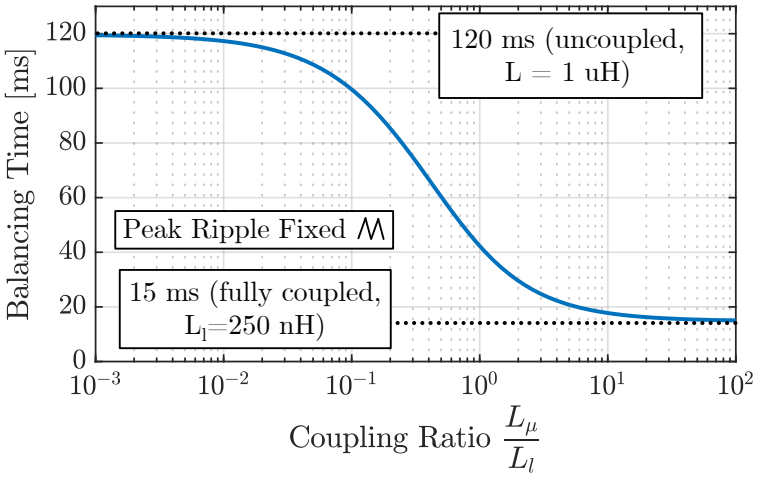


Figure 3.10: PLECS simulation of balancing time vs. coupling ratio with parameters in Section 3.3, with maximum per-phase current ripple fixed.

an eight-phase example. With a common-mode imbalance, the imbalance current and associated loss are large, which causes faster balancing. With a differential-mode imbalance, the switch node voltage constantly alternates, keeping the imbalance current and loss small, making the converter balance slower. Common-mode imbalances excite the leakage inductance and differential-mode imbalances excite the magnetizing inductance, which we is much larger for tightly coupled inductors [5]. The current is therefore much larger and lossier in the former case. As found before, only the one- and two- phase converters have a single balancing mode. Adding more phases introduces uncertainty in the balancing time depending on the imbalance. In the case that this uncertainty is undesirable, it would be better to use only a two-phase coupled inductor converter.

The slowest and fastest balancing modes predicted by the state-space model for for multiphase converters is shown in Fig. 3.9, where the maximum ripple current is kept constant between circuits. The slowest and fastest balancing time constants bound the possible balancing times, and other modes exist between them. The only converters with a deterministic balancing time are the one- and two-phase converters. In summary, the state-space model of coupled inductor FCML balancing dynamics shows the multi-resonant balancing properties dependent on the initial condition, and how slow and fast initial conditions can be predicted from the resultant loss.

Table 3.4: Circuit Parameters of the FCML Prototype

Parameter/Component	Value
f_{sw}	500 kHz
V_{dc}	16 V
C_{fly}	1206 10 μF $\times$ 2
Custom Coupled Inductor L_l	23 & 192 nH
Custom Coupled Inductor L_μ	230 & 7.44 uH
Two-phase Coupled Inductor	Coilcraft PA6605-AL
Discrete Inductor	Coilcraft XAR7030-222MEB
Switches	EPC2067
Controller	EP4CE15F23C8

3.4.3 Model Limitations

The two balancing models presented in this work cover many common FCML converters, but they have some important limitations. First, the power dissipation model, while useful for relating the loss-context and balancing dynamics, only works in special circumstances where the loss is dependent only on the total normalized imbalance and not the specific imbalance in each flying capacitor. As mentioned before, this precludes its use for larger-order multi-resonant converters.

The state-space model is applicable to all converter sizes, but it suffers from elevated computational complexity and a lack of closed-form solutions. Additionally, the model assumes highly coupled inductors with high quality factor to simplify the calculations. As shown in [72], steady-state balancing analysis of fully-coupled inductors largely applies to moderately coupled inductors, with a smooth transition to the uncoupled solution. This occurs because even moderately coupled inductors share most of the inductive characteristics of fully coupled inductors. Fig. 3.10 shows the simulated balancing time of a two-phase, three-level FCML converter with varying coupling ratio and the peak ripple fixed. At the coupling extremities, the results match the model derived in Section 3.3. The balancing time is similar to the fully-coupled solution even with moderate coupling ratios under $\frac{L_\mu}{L_l} < 10$.

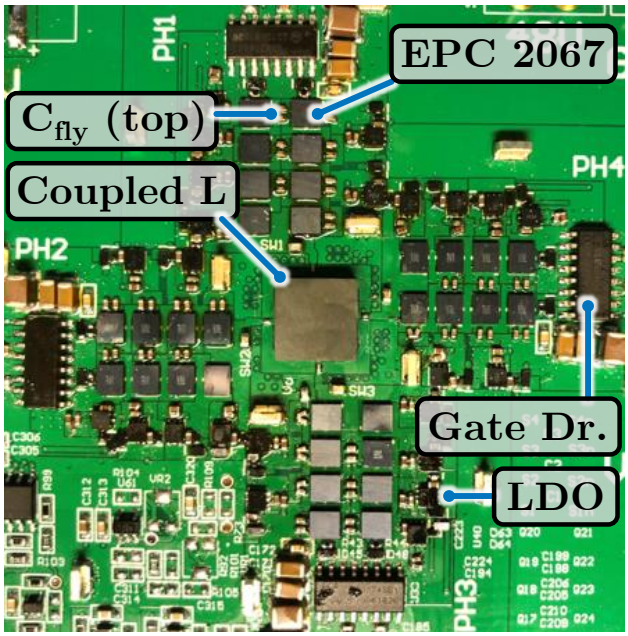


Figure 3.11: Picture of the four-phase five-level FCML prototype with a four-phase coupled inductor implemented with PCB windings.

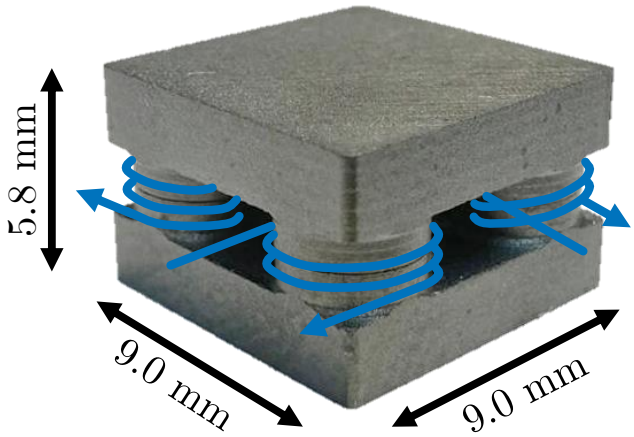


Figure 3.12: Four-phase coupled inductor core using DMR53 material. The core consists of two identical halves pressed together from both sides of the PCB; the three-turn windings are formed by the PCB traces.

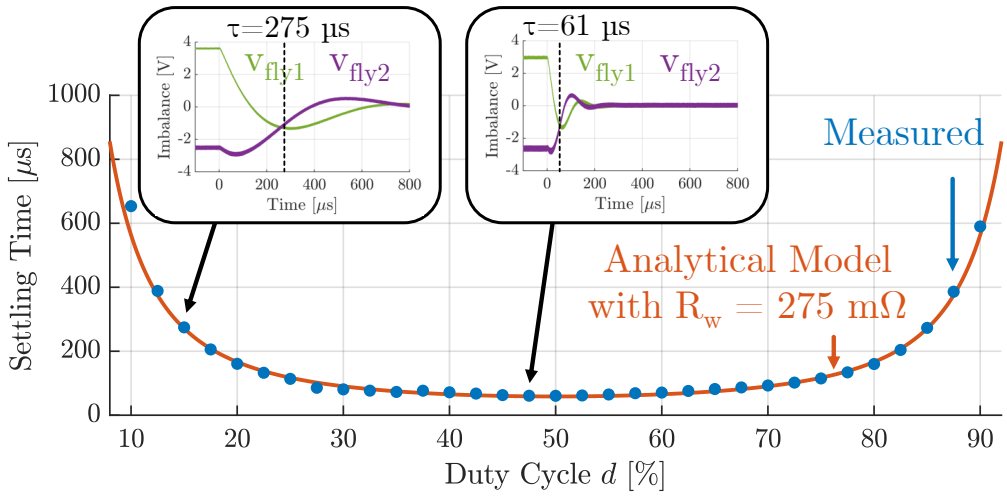


Figure 3.13: Measured balancing time of a two-phase, three-level FCML converter compared to the power dissipation theoretical model. Each measured point represents a measurement of the time taken for the normalized imbalance to reduce to $e^{-1}\times$ the starting value.

3.5 Experimental Verification

To verify the theoretical balancing dynamics across converters with different numbers of phases, levels, switching frequencies, and coupling properties, we use the prototype shown in Fig. 3.11. The circuit parameters and components are listed in Table 3.4 and the coupled inductor design is shown in Fig. 3.12. To introduce an initial imbalance, the phase shift between switches are deviated from their nominal values. This disturbance forces an imbalance voltage on the flying capacitors that depends on the phase shift applied to each phase [38, 66]. The disturbances are removed at time $t = 0$ and the flying capacitors dynamically balance to their nominal values. The balancing time is defined as the time taken for the normalized imbalance $\|\tilde{\mathbf{v}}_{\text{fly}}\|$ to decay to $e^{-1}\times$ of its starting value.

First, we verify the power dissipation model by measuring the balancing time of the two-phase, three-level converter with tightly coupled inductors and comparing it to the equation derived in eq. (3.22). The inductance, capacitance, switching frequency, and duty cycle are known or readily measured, but the effective R_w generating loss from the imbalance is not. To estimate R_w, we compare the power dissipated in the converter with and without an external imbalance. From here, we estimate the effective resistance that captures the imbalance-based loss

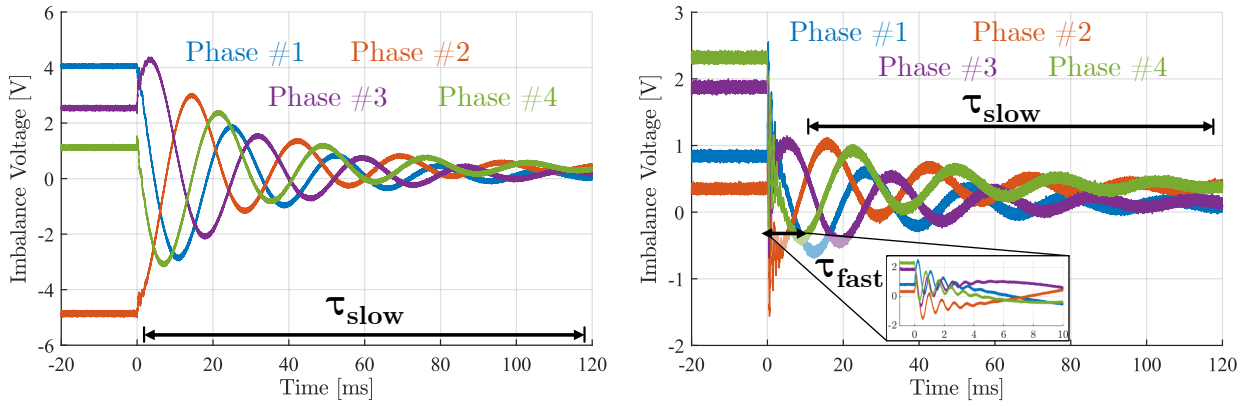
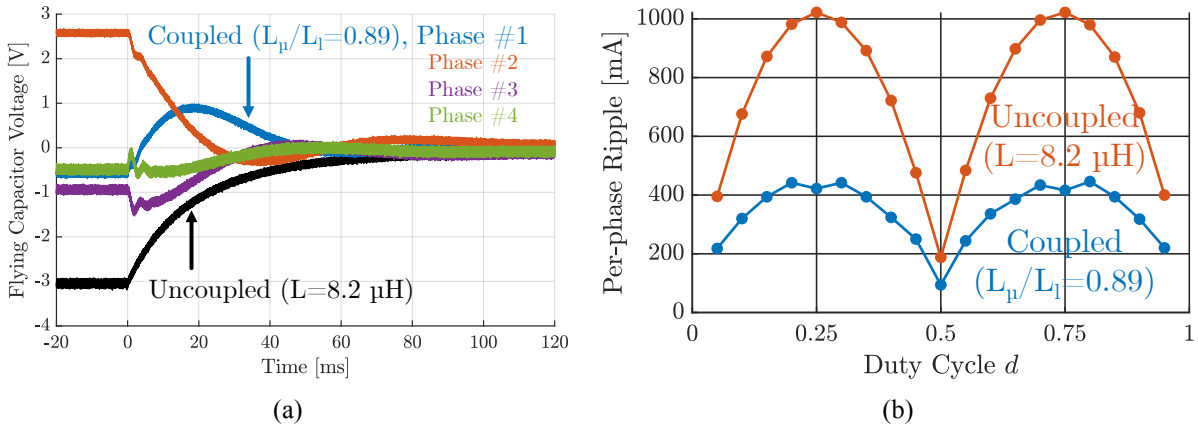


Figure 3.14: Dynamic balancing of flying capacitors with initial conditions created by timing delays (a) $\mathbf{t}_1 = \{73, 1, -87, 57\}$ ns and (b) $\mathbf{t}_2 = \{-90, -100, -48, 65\}$ ns. Depending on the initial conditions, the voltages resonate with different frequencies and decay speeds.

is $R_w = 275$ mΩ. At each duty cycle in Fig. 3.13, the balancing time is measured and plotted against the analytical model with a good match.

Next, we verify the multi-resonant properties of a four-phase, three-level FCML converter with tightly coupled inductors. Fig. 3.14 shows balancing from two different initial conditions caused by external disturbances: (a) a time delay of $\mathbf{t}_1 = \{73, 1, -87, 57\}$ ns for phases #1 through #4, and (b) $\mathbf{t}_2 = \{-90, -100, -48, 65\}$ ns. The first imbalance almost exclusively contains components of the slowly decaying mode. The second imbalance contains components of both the fast and slow modes. The fast mode decays rapidly and oscillates at a high frequency. The difference between the two time constants is significant.

Even loosely or moderately coupled inductors still yield major improvements in ripple, transient response, and size, while having greater robustness to single-phase failure than tightly coupled inductors. Similarly, the dynamic balancing behavior changes depending on the coupling ratio. Fig. 3.15(a) shows the flying capacitors balancing from an initial imbalance created by a uniform delay of -140 ns in each phase. The uncoupled inductors have $L = 8.2$ μH and switching frequency is reduced to 100 kHz. The coupled inductors have similar leakage inductance and a coupling ratio $\frac{L_\mu}{L_l} = 0.89$, significantly lower than the tightly coupled inductors used before. As a result, the oscillations are damped and the flying capacitors balance quickly. The time constant



(a) (b)

Figure 3.15: (a) Flying capacitor balancing and (b) ripple of four-phase FCML converter with f_{sw} = 100 kHz. With loosely coupled inductors, the dynamic balancing is damped and the ripple is reduced compared to uncoupled inductors with inductance L = 8.2 μH equal to the leakage inductance.

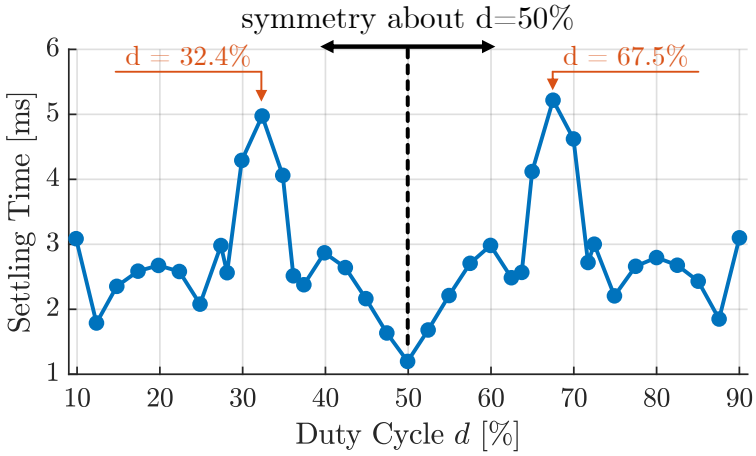
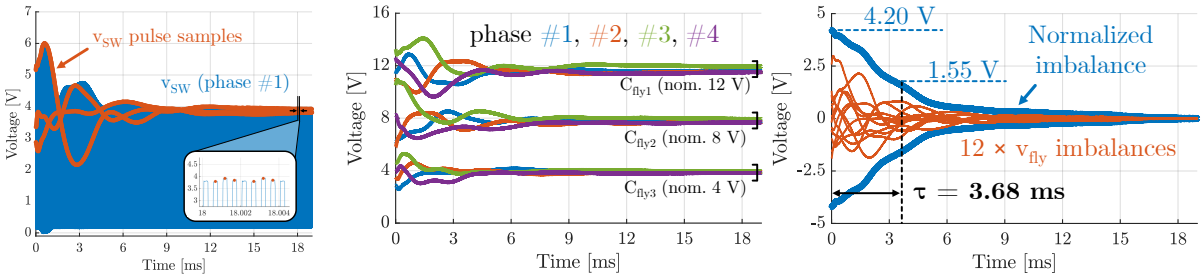


Figure 3.16: Balancing time of normalized imbalance of four-phase converter across duty cycle range.



(a) (b) (c)

Figure 3.17: (a) Raw switch node voltage measurement and sampling, (b) inference of flying capacitor voltages from switch node samples, and (c) conversion to imbalance components and normalized imbalance.

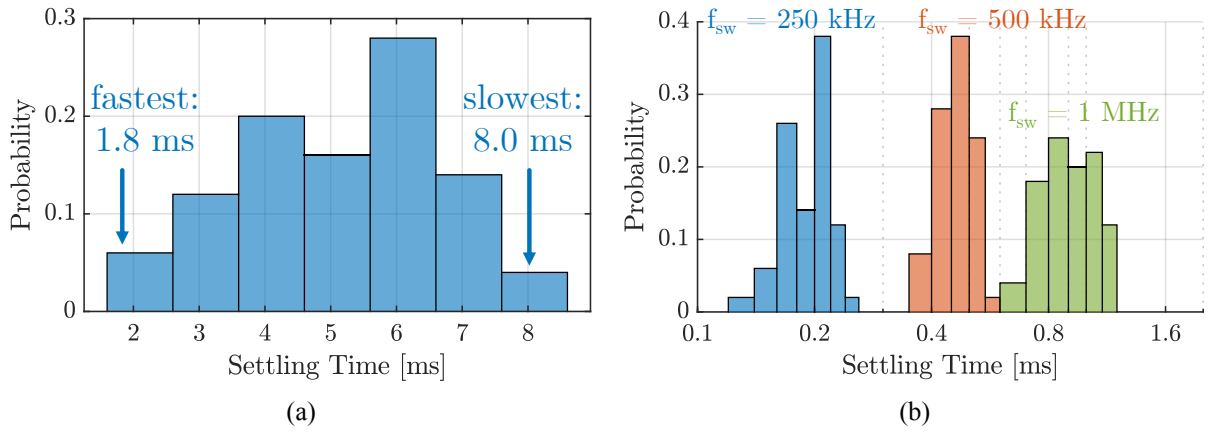


Figure 3.18: (a) Histogram of experimentally measured balancing time at $d = 0.125$ and (b) with different switching frequencies.

is similar to the uncoupled inductors since the leakage inductance is also approximately 8.2 μH. Fig. 3.15(b) shows the average per-phase ripple current of the uncoupled and loosely coupled converters. Therefore, the partially coupled inductors can simultaneously improve the ripple and steady-state imbalance without negatively affecting the balancing speed so long as the leakage inductance is kept constant.

Across the duty cycle range, the balancing time of a four-phase converter has a more complex trend, as shown in Fig. 3.16. The balancing time is still symmetric about $d = 0.5$, and two outlying points are aligned with singularities of coupled inductor balancing of four-phase converters [72].

As the number of phases, levels, and flying capacitors increases, the complexity of the balancing dynamics increases. To measure the 12 flying capacitor voltages for our four-phase, five-level prototype, we estimate them from the voltage pulses at the switch nodes. This is illustrated in Fig. 3.17(a). Like with the four-phase, three-level case, the capacitors start imbalanced and then oscillate to their balanced levels at $1/4$, $1/2$, and $3/4$ of the input voltage, as shown in Fig 3.17(b). Finally, we find the balancing time in Fig. 3.17(c).

We use Monte Carlo analysis to study the balancing dynamics of the larger converter. In Fig. 3.18(a), the converter is operated at $f_{sw} = 500$ kHz and $d = 0.125$ with a random phase shift being applied to each of the set of switches between $\pm 7.2°$ over 50 trials. Due to the multi-

resonance of the converter, the balancing time varies widely between 1.8 ms and 8 ms. The initial conditions significantly impact how fast a coupled FCML converter balances. Next, Fig. 3.18(b) shows the distribution of balancing times with the converter operating at $d = 0.375$ and three switching frequencies, with the same random phase shift on each set of switches. The balancing time again varies widely from minimum to maximum, and the balancing time increases as the frequency increases. This verifies the scaling of balancing time with frequency, and more fundamentally, the fact that balancing depends on the magnitude of loss that the imbalance generates.

3.6 Chapter Summary

This chapter develops dynamic models for coupled inductor FCML converter balancing. A model based on power dissipation is used for simple FCML converters to produce closed-form results that emphasize the importance of the loss-context on the balancing speed. A generalized state-space model is extended for coupled inductors of any number of phases and levels that reveals the multi-resonant behavior of FCML converter balancing, where the initial conditions determine the speed of balancing. Finally, the theoretical models are verified with detailed dynamic balancing experiments on FCML prototypes with varying switching frequencies, inductances, and numbers of phases and levels.

4

Achieving an Order-of-Magnitude Scale-Up of Balanced Frequency Multiplication

The contents of this chapter were previously published under D. H. Zhou, K. Manos, and M. Chen, IEEE Applied Power Electronics Conference (APEC), 2025.

Abstract

This chapter combines multiphase and multilevel interleaving using distributed active switches and integrated magnetics into a unified very large scale interleaving (VLSI) technique to develop ultra-fast power electronics with outstanding large-signal tracking capability. The large-signal reference-tracking capabilities considering the fundamental sampling limit, modulator, and output filter are derived, including how reduced-amplitude, above-switching-frequency tracking is possible for highly interleaved converters. The capabilities of very large scale interleaving are demonstrated with a 64× interleaved, four-phase, 17-level FCML converter enabled by passive flying capacitor balancing provided by a four-phase tightly coupled inductor. The applicability and efficacy of the theory are verified by using the converter to directly power a 400 W Li-Fi transmitter communicating with OOK/16-QAM at 2.4× the switching frequency and 95.5% efficiency.

4.1 Chapter Introduction

Multiphase interleaving, multilevel interleaving, and coupled magnetics [22, 26, 30, 57, 69] are important techniques that extend the capabilities of PWM (pulse-width-modulated) converters in high-speed applications such as envelope tracking [74, 75] and communication-over-power [14, 76]. In particular, interleaved power converters can be of benefit for Li-Fi (Light Fidelity) [77, 78], as they can provide high efficiency power delivery and fast modulation for LED illumination. Multiphase and multilevel interleaving multiply the effective switching frequency of the current and voltage ripples in the converter, reducing loss and the required passive component sizes [25]. Multiphase converters can also take advantage of coupling the magnetics [26], while multilevel topologies such as the FCML (flying capacitor multilevel) converter [30] can yield major efficiency and density benefits by replacing inductor volume with energy-dense capacitors and interleaved switches [25, 79, 80]. This has motivated FCML converters with many levels [50, 51, 53] and variations which also leverage multiple phases and coupled inductors [71, 72].

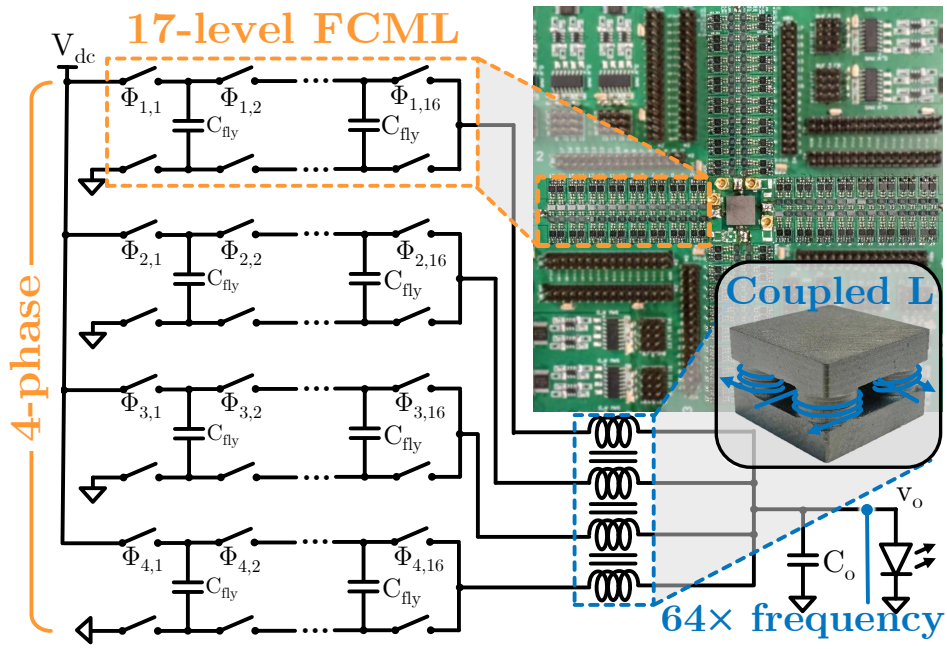


Figure 4.1: Four-phase, 17-level coupled inductor FCML converter schematic.

However, major obstacles remain with interleaved FCML converters: first, the flying capacitors must be balanced to maintain an undistorted output and appropriate switch voltage stress [34, 36], which is challenging with many levels and higher switching frequencies. Second, the output voltage tracking capabilities of interleaved converters are not fully understood beyond half the switching frequency [81–83], at beat-frequency harmonics [84–86], and with nontraditional PWM carriers [87, 88]. In particular, the relation between the switching frequency, effective switching frequency, and maximum output tracking frequency is not clear at present.

This chapter presents several contributions to the theory and application of interleaved power electronics: (i) a unification of multilevel and multiphase interleaving together with coupled magnetics as a very large scale interleaving (VLSI) technique in power electronics, (ii) a complete theory on the large-signal tracking capabilities of open-loop interleaved converters, (iii) a 64× interleaved, four-phase, 17-level coupled inductor FCML converter (Fig. 4.1) pushing the experimental limits of interleaved switching, (iv) an application of large-scale coupled inductor FCML balancing, and (v) a demonstration of advanced communication-over-power at 2.4× the switching frequency on a directly-powered 400 W Li-Fi transmitter.

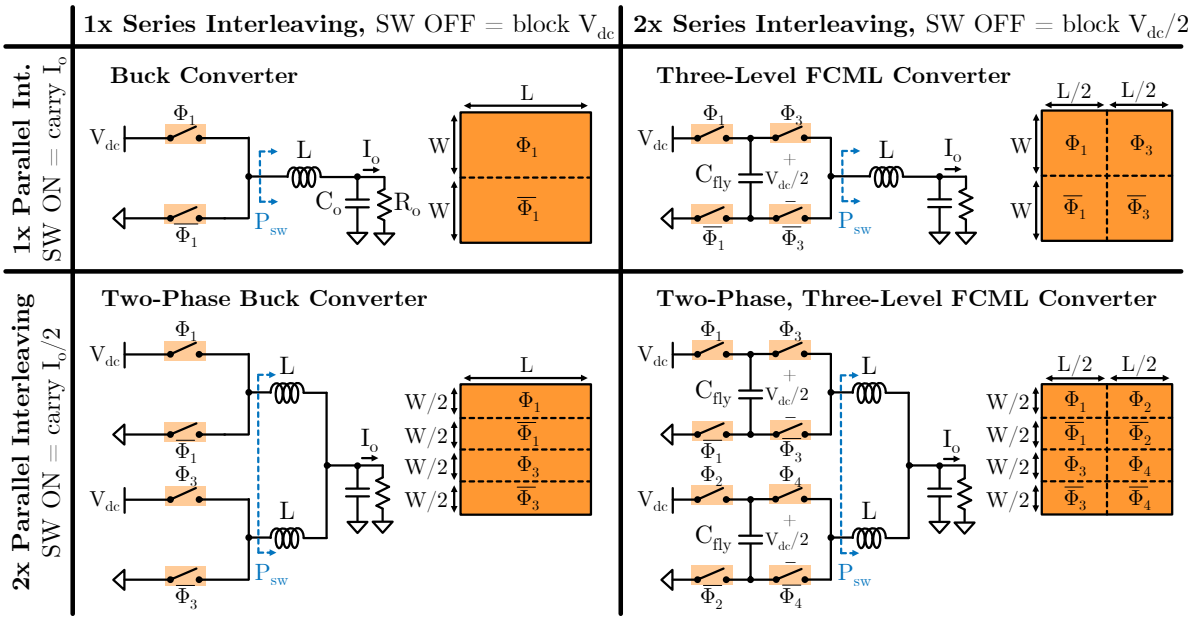


Figure 4.2: Chart of switch areas (Φ denoting gate signals) and example schematics of converters with parallel interleaving, series interleaving, and a combination.

4.2 Very Large Scale Interleaving Power Electronics (VLSI-PE)

Interleaving fundamentally involves splitting one switch into more than one and driving those switches with phase-shifted gate signals. This can be done by putting multiple switches in parallel, such as with the multiphase buck converter, or in series, such as with FCML converters. In this section, we unify these two interleaving concepts under the assumption that the total switch area is fixed and all switches have the same size. Our base case is a buck converter with two equally sized switches with width W and length L. When one of the switches is on, it carries the full inductor current, which has an average of I_o. When off, it blocks the full input voltage, V_{dc}. The total switch area is $2WL$.

The voltage-blocking and current-carrying capability of a switch are proportional to its length and width respectively. Ideally, we can divide the total switch area $2WL$ into multiple narrower devices in parallel or shorter devices in series and handle the same V_{dc} and I_o so long as each carries a current and blocks a voltage proportional to its width and length. This is shown in Fig. 4.2 with the two-phase buck converter and three-level FCML converter, or a combination of both multiphase and multilevel switching at once. If we then phase shift the gates, we multiply the

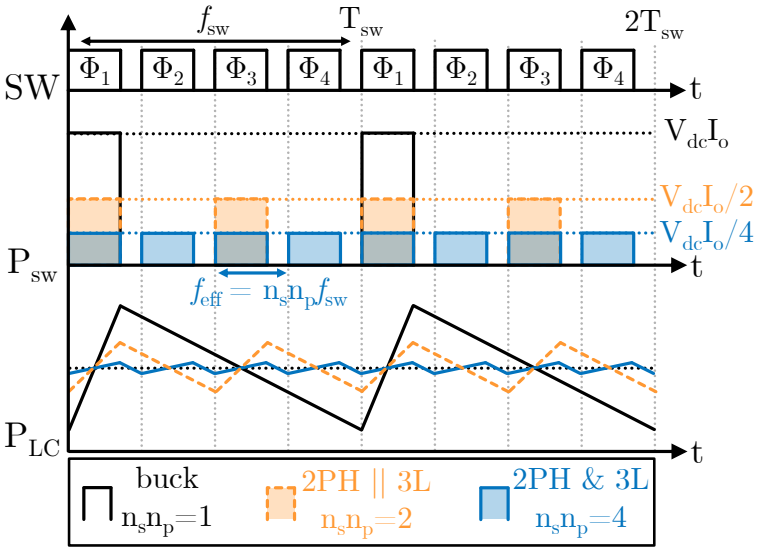


Figure 4.3: Power flow waveforms of the four converters in Fig. 4.2. Interleaving increases the frequency of pulses and reduces their amplitude, reducing the level of energy that must be stored in the inductor and capacitor.

effective switching frequency of the converter without changing the switch area. We define the series and parallel interleaving factors n_s and n_p as the number of top-side switches in series and parallel respectively. We then index the $n_s n_p$ top-side switches by their phase $p = 1, \ldots, n_p$ and their position in series $s = 1, \ldots, n_s$, where the switch closest to the input is $s = 1$. The switches are driven with uniformly phase-shifted PWM signals with phase shift

$$\theta_{sp} = \theta_k = k\frac{2\pi}{n_s n_p}, \tag{4.1}$$

where $k = (p-1) + (s-1)n_p$ indexes the switches from $k = 0$ to $k = n_s n_p - 1$ by the order of their phase shift. The effective switching frequency of an interleaved converter with uniform phase shifting is

$$f_{\text{eff}} = n_s n_p f_{\text{sw}} = N f_{\text{sw}}, \tag{4.2}$$

where $N = n_s n_p$ is the total interleaving factor of the converter. Since the two interleaving techniques are dividing different things (voltage or current), we now examine how interleaving divides power flow. Assuming the currents and blocking voltages are balanced, the inductor cur-

rent carried by each phase is I_o/n_p and the switch node voltage of each phase is equal to the number of switches turned on in that phase multiplied by the blocking voltage. The power transferred to the output network as labeled in Fig. 4.2 is

$$\begin{aligned} P_{\text{sw}} = \sum_{p=1}^{n_p} v_{\text{sw},p} \times i_{L,p} &= \sum_{p=1}^{n_p} \left(\frac{I_o}{n_p} \times \sum_{s=1}^{n_s} \Phi_{sp} \frac{V_{\text{dc}}}{n_s} \right) \\ &= \frac{I_o V_{\text{dc}}}{n_p n_s} \sum_{p=1}^{n_p} \sum_{s=1}^{n_s} \Phi_{sp} \\ &= \frac{I_o V_{\text{dc}}}{N} \sum_{k=0}^{N-1} \Phi_k = \frac{I_o V_{\text{dc}}}{N} \times n_{\Phi=1}, \end{aligned} \tag{4.3}$$

where $n_{\Phi=1}$ is the number of top switches that are turned on. Eq. (4.3) shows that interleaving divides the maximum input power, $I_o V_{\text{dc}}$, into N equal divisions controlled by the N top switches. Eq. (4.2) and (4.3) quantify the key benefit of interleaving: ideally, **we can split the same switch area into smaller switches that divide the power flow into steps controlled with greater granularity and at a higher frequency.** This is illustrated in Fig. 4.3. For the one-phase buck converter, $N = 1$ and there is only one switch which delivers the maximum input power $V_{\text{dc}} I_o$ when it is on, and none otherwise, with energy storage components handling the balance. An interleaved converter can switch between power levels much closer to the load at a greater frequency, reducing the required energy storage. Note that an interleaved converter only divides power flow control, but does not change the maximum or minimum power flow. Even if all the switches of an interleaved converter are turned on or off, the minimum and maximum power transferred to the load is still the same as a buck converter. Since we often wish to track a particular output voltage, we define the effective switch node voltage as

$$v_{\text{sw,eff}} = \frac{V_{\text{dc}}}{N} \times n_{\Phi=1}, \tag{4.4}$$

taken from eq. (4.3). We use $v_{\text{sw,eff}}$ to track a reference signal and filter it with the L-C output filter. The effective switch node voltage reformulates the power divisions in (4.3) as voltage divisions, even if there may physically be multiple switch nodes in the multiphase converter.

4.3 The Large-Signal Reference-Tracking Limits of Open-loop VLSI-PE Converters

The Nyquist sampling theorem, in its most common form, states that if a signal is sampled *"at a rate slightly higher than twice the highest significant signal frequency, then the samples contain all of the information of the original signal"* [89], making signal reconstruction possible with an ideal low-pass filter (LPF). Interleaved power converters bear many similarities to the communication systems for which this principle was originally written; we modulate a reference signal to drive PWM switches and recover the desired signal and attenuate the switching harmonics with an L-C filter. In this section, we adapt the Nyquist sampling principle and other elements of modulation theory to answer the following question: how do the switching frequency and effective switching frequency determine the signal-tracking capability of an interleaved converter? We find that interleaving **splits one large control action into smaller ones at a higher frequency, improving large-signal reference tracking resolution and range**, albeit at a reduced amplitude. We assume that the converter is balanced and has ideal phase shifts.

4.3.1 The Sampling Principle Adapted to Interleaved Converters

First, we adapt the sampling principle above while assuming an ideal modulator and LPF to derive the fundamental tracking limit. We assume that the reference signal is

$$v_{\text{ref}}(t) = \frac{A_{\text{ref}}}{2} + \frac{A_{\text{ref}}}{2}\cos(2\pi f_{\text{ref}} t), \tag{4.5}$$

with peak-to-peak amplitude A_{ref}, frequency f_{ref}, and period $T_{\text{ref}} = \frac{1}{f_{\text{ref}}}$, which we seek to track as closely as possible with $v_{\text{sw,eff}}$. With a fixed switching frequency f_{sw}, the N switches are turned on and off once per $T_{\text{sw}} = \frac{1}{f_{\text{sw}}}$, with each switching event increasing or decreasing the effective switch node voltage by $\frac{V_{\text{dc}}}{N}$. The two frequency ranges of interest are:

(i) $f_{\text{ref}} \leq f_{\text{sw}}$: a large-N interleaved converter can track a sub-f_{sw} reference signal with any amplitude $A_{\text{ref}} \leq V_{\text{dc}}$, as illustrated in Fig. 4.4 assuming the switching events happen at uniform

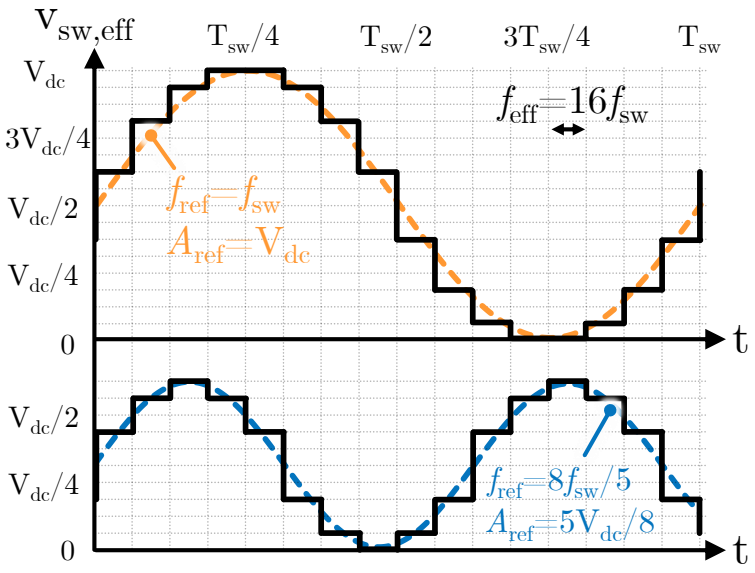


Figure 4.4: A $N = 16\times$ interleaved converter with ideal PAM-approximating level-selection tracking reference signals at the output-slope limit.

times separated by T_{eff}. This is because in time T_{sw}, the reference signal will traverse, at most, from zero to V_{dc} and back once. In the same time, we are able to turn on and off every switch once and traverse the same amplitude with $v_{\text{sw,eff}}$. If N is high, the interleaved converter can output levels very close to v_{ref} for each time segment T_{eff}, as shown in Fig. 4.4, allowing signal recovery from $v_{\text{sw,eff}}$ through the LPF.

(ii) $f_{\text{sw}} \leq f_{\text{ref}} \ll f_{\text{eff}}$. If we let $f_{\text{ref}} = \frac{f_{\text{eff}}}{\rho}$, where $\{\rho \in \mathbb{R} \mid 1 \ll \rho \leq N\}$, we can turn on and off at least $[\text{floor}(\rho)]$ switches in time T_{ref}, so the output of the converter can track a signal with peak-to-peak amplitude up to $A_{\text{ref}} \leq \frac{\text{floor}(\rho)}{N} V_{\text{dc}}$. This is illustrated in Fig. 4.4 for $\rho = 10$: the $N = 16$ converter can track a signal with frequency $f_{\text{ref}} = \frac{f_{\text{eff}}}{10} = \frac{8f_{\text{sw}}}{5}$ up to amplitude $A_{\text{ref}} = \frac{5V_{\text{dc}}}{8}$. If we substitute the reference frequency into the maximum amplitude expression, we derive the inequality

$$A_{\text{ref}} f_{\text{ref}} \leq \frac{\text{floor}(\rho)}{\rho} V_{\text{dc}} f_{\text{sw}}, \tag{4.6}$$

the fundamental output tracking limit of an interleaved converter for $f_{\text{sw}} \leq f_{\text{ref}} \ll f_{\text{eff}}$. Both sides of the inequality (4.6) are in units [volts/time], making it interpretable as a restriction on the

maximum large-signal slope of the reference signal. Essentially, the voltage traversal or average slope of the reference signal, $A_{\text{ref}} f_{\text{ref}}$, must not be greater than what the converter can fundamentally provide, $V_{\text{dc}} f_{\text{sw}}$, with a possible reduction if $\rho \notin \mathbb{Z}$ because of the finite number of levels. This relates to section 4.2; interleaving multiplies the frequency of control actions, but also proportionally divides their amplitude.

If the reference signal frequency and amplitude requirements are at the limits above (equality case in (4.6)), the maximum frequency may be limited by the quantization error introduced by the finite number of levels. An interleaved converter in this regime acts similarly to a pulse amplitude modulation (PAM) system, which samples a waveform and outputs pulses of modulated amplitude instead of width like in PWM. As shown in [89], a PAM system can be used to exactly represent a signal by taking regular samples and extending them into an array of flat-top pulses of duration T_{eff}, then passing the result through an ideal LPF to result in

$$v_{\text{o,LPF}} = \operatorname{sinc}\left(\frac{\pi f_{\text{ref}}}{f_{\text{eff}}}\right) \frac{A_{\text{ref}}}{2} \left(1 + \cos\left[2\pi f_{\text{ref}} \left(t - \frac{T_{\text{eff}}}{2}\right)\right]\right), \tag{4.7}$$

adapted from eq. (4-1) of [89], meaning the original signal is recovered perfectly, albeit with a phase shift and attenuation factor. Although we do not conduct a detailed investigation of the effect of quantization on reference tracking here, we note that as long as the effective switching frequency of the converter is much higher than the reference frequency, the converter can represent a reference signal well, allowing it to be reconstructed like in a PAM system.

4.3.2 Large-Signal Slope and Harmonic Limit of the Modulator

The reference signal is typically modulated with a triangle or sawtooth carrier wave to generate the PWM waveforms, and the slope of the carrier limits the maximum slope of the reference signal. For non-interleaved converters, the reference signal frequency and slope tend to be much lower than the carrier waveform. Interleaved converters may track signals near or above the switching frequency, so we must consider the carrier slope restriction. The PWM waveform is typically generated by comparing the reference $v_{\text{ref}}(t)$ to the carrier:

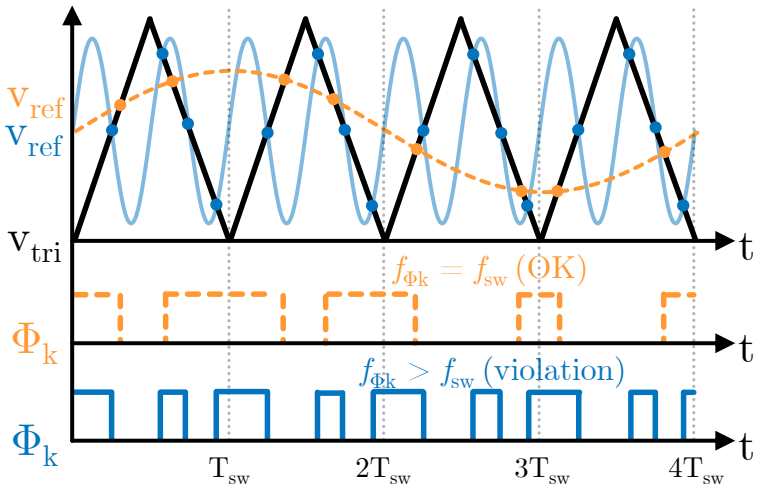


Figure 4.5: PWM signal generation with reference signal below and above the slope limit, producing PWM signals with correct and excessive frequency.

$$\Phi_k(t) = \begin{cases} 1 & v_{\text{ref}}(t) \geq v_{\text{carrier},k}(t) \\ 0 & v_{\text{ref}}(t) < v_{\text{carrier},k}(t) \end{cases}, \tag{4.8}$$

where $v_{\text{carrier},k}(t)$ is the carrier for the kth switch with phase shift defined in (4.1). The carrier wave is periodic with the switching frequency f_{sw}, ramping up and down with slope $\frac{2V_{\text{dc}}}{T_{\text{sw}}}$ with a triangle carrier or slope $\frac{V_{\text{dc}}}{T_{\text{sw}}}$ up (trailing-edge) or down (leading-edge) with a sawtooth carrier. The reference signal should intersect with the carrier twice per period, as illustrated with the dotted v_{ref} in Fig. 4.5, such that v_{PWM} turns on once and off once per period. This is guaranteed if the maximum slope of v_{ref} is less than the slope of the carrier. From eq. (4.5), the maximum slope of the signal is is $\pi \mathcal{A}_{\text{ref}} f_{\text{ref}}$, so the modulator restricts the large-signal reference to

$$\mathcal{A}_{\text{ref}} f_{\text{ref}} \leq \begin{cases} \frac{2}{\pi} V_{\text{dc}} f_{\text{sw}}, & \text{triangle carrier} \\ \frac{1}{\pi} V_{\text{dc}} f_{\text{sw}}, & \text{sawtooth carrier} \end{cases} \tag{4.9}$$

The modulator restricts the slope of the reference signal below the theoretical maximum (4.6). If the slope of the reference signal exceeds the carrier, such as with the solid reference signal in Fig. 4.5, the PWM signal frequency will exceed the desired switching frequency or be distorted if latched. Thus far, we have only derived the large-signal slope restriction for valid PWM, but we

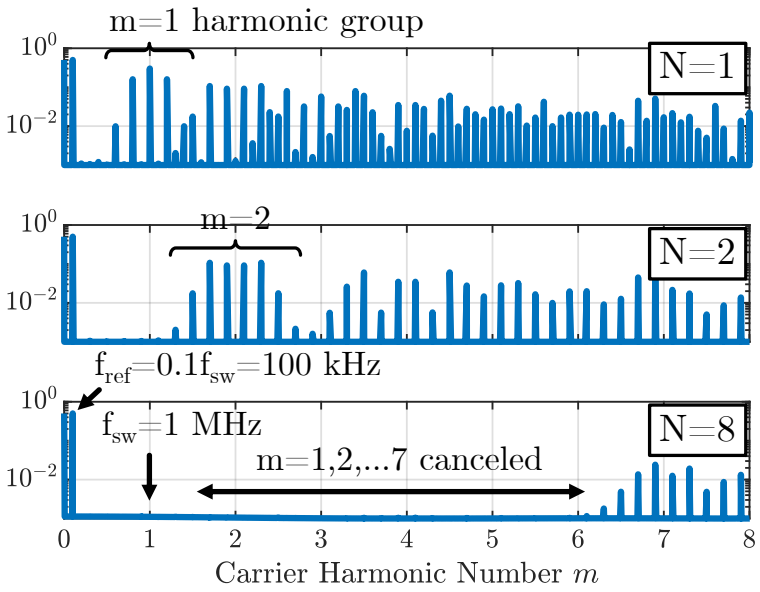


Figure 4.6: Spectrum of $v_{\text{sw,eff}}$ for interleaved converters with $f_{\text{sw}} = 1$ MHz, $f_{\text{ref}} = 100$ kHz, and $V_{\text{dc}} = 1$ V. Harmonics up to $m = N - 1$ are canceled.

have not yet shown that the output will track the reference signal correctly. To do so, we study the spectrum of the effective switch node voltage from eq. (4.4)

$$
\begin{aligned}
v_{\text{sw,eff}}(t) = \frac{V_{\text{dc}}}{N}\sum_{k=0}^{N-1}\Phi_k(t) = \underbrace{\frac{A_{\text{ref}}}{2}}_{\text{dc component}} + \underbrace{\frac{A_{\text{ref}}}{2}\cos(\omega_{\text{ref}}t)}_{\text{desired reference signal}} \\
+ \underbrace{\sum_{m=1}^{\infty}\frac{4V_{\text{dc}}J_0\left(mM\frac{\pi}{2}\right)\sin\left(m\frac{\pi}{2}\right)}{N\pi m}\times\underbrace{\sum_{k=0}^{N-1}\cos\left(m\omega_{\text{sw}}t + m\theta_k\right)}_{\alpha}}_{\text{carrier harmonics}} \\
+ \underbrace{\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{4V_{\text{dc}}\sin\left((m+n)\frac{\pi}{2}\right)}{N\pi}\times\underbrace{\sum_{k=0}^{N-1}\cos\left((m\omega_{\text{sw}} + n\omega_{\text{ref}})t + m\theta_k\right)}_{\beta}}_{\text{sideband harmonics}}
\end{aligned}
\tag{4.10}
$$

with a triangle carrier as adapted from (3.39) of [90], where ω_{sw} and ω_{ref} are the angular switching and reference frequencies and $M = \frac{A_{\text{ref}}}{V_{\text{dc}}}$ is the modulation ratio. The Fourier series consists of four parts: a desired dc component, a desired modulated component at the reference frequency, and the undesired carrier and sideband harmonics. The carrier harmonics occur at multiples m of the switching frequency f_{sw} and sideband harmonics occur around the carrier harmonics at

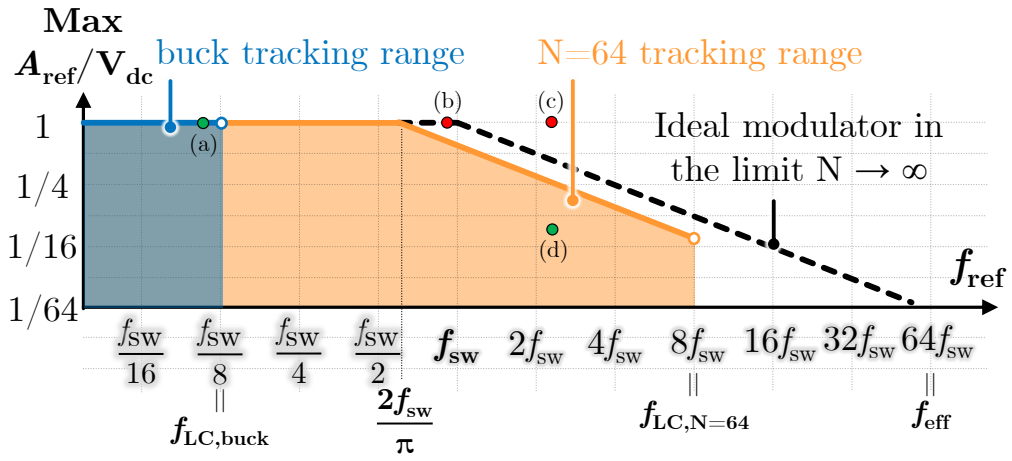


Figure 4.7: Plot of maximum reference amplitude vs. reference frequency of a $N = 64\times$ interleaved converter compared to a buck converter. The points (a) through (d) denote reference signals tracked in the experimental section.

multiples n of the reference frequency f_{ref}. The harmonic magnitudes decrease as m and n increase. Since there are an infinite number of sideband harmonics of a PWM signal, there is no strict boundary between acceptable and unacceptable distortion for signal reconstruction. Instead, the signal is considered well-represented by a PWM signal if the dominant sideband and carrier harmonics are far enough from f_{ref} to be filtered by the LPF to a negligible level and the smaller magnitude harmonics are ignored. Since the first group of harmonics occurs at and about the switching frequency, we must prove that interleaved converters cancel carrier and sideband harmonics if we wish to track reference signals around or above f_{sw}.

The expressions α and β in eq. (4.10) are sums of N cosines for the carrier and sideband harmonics produced by each PWM, except with a different phase shift θ_k for each term. If $\alpha = 0$ or $\beta = 0$ for a given carrier or sideband harmonic, then that harmonic will be canceled. We consider that

$$\sum_{k=0}^{N-1} \cos(x + m\theta_k) = \sum_{k=0}^{N-1} \frac{\left(e^{j(x+m\theta_k)} + e^{-j(x+m\theta_k)}\right)}{2} \tag{4.11}$$

$$= \frac{e^{jx}}{2} \sum_{k=0}^{N-1} \left(e^{jm\frac{2\pi}{N}}\right)^k + \frac{e^{-jx}}{2} \sum_{k=0}^{N-1} \left(e^{-jm\frac{2\pi}{N}}\right)^k \tag{4.12}$$

$$= \frac{e^{jx}}{2} \frac{1 - \cancelto{0}{e^{jm2\pi}}}{1 - e^{jm\frac{2\pi}{N}}} + \frac{e^{-jx}}{2} \frac{1 - \cancelto{0}{e^{-jm2\pi}}}{1 - e^{-jm\frac{2\pi}{N}}} = 0, m \notin N\mathbb{Z}, \tag{4.13}$$

where we expand the cosine terms with Euler's identity in (4.11), apply the geometric series in (4.12) for any non-integer ratio $\frac{m}{N}$, and note that the numerators cancel to zero for any valid m in (4.13). Therefore, for any m from $m = 1$ to $m = N - 1$, the sum of cosines in (4.11) sums to zero. Since expressions α and β of eq. (4.10) are in the form of eq. (4.11), we conclude that the carrier and sideband harmonics of an $N\times$ interleaved converter at and about the first $N-1$ carrier harmonics all cancel out. The lowest frequency non-canceled harmonics occur at the effective switching frequency, as verified in Fig. 4.6.

The preceding result also shows how interleaving allows the use of an smaller L-C filter with a higher cutoff frequency. The L-C cutoff frequency, which needs to be set far below the switching frequency in a buck converter, may now be set relative to the effective switching frequency. The analysis is limited since practical phase shifting is affected by factors like propagation delay, which will lead to imperfect cancellation of undesired harmonics. Additionally, the fact that $f_{\text{eff}} = Nf_{\text{sw}}$ does not mean we can track a reference signal $N\times$ faster than a buck converter, because the sideband harmonics are located about the carrier harmonics at integer multiples of the reference frequency. Therefore, as the reference frequency increases, the sidebands (especially those with a higher order n) will approach the in-band frequencies passed by the LPF. Finally, we do not address beat-frequency harmonics or intrinsic unbalancing of interleaved converters when the reference frequency is an exact multiple of the switching frequency.

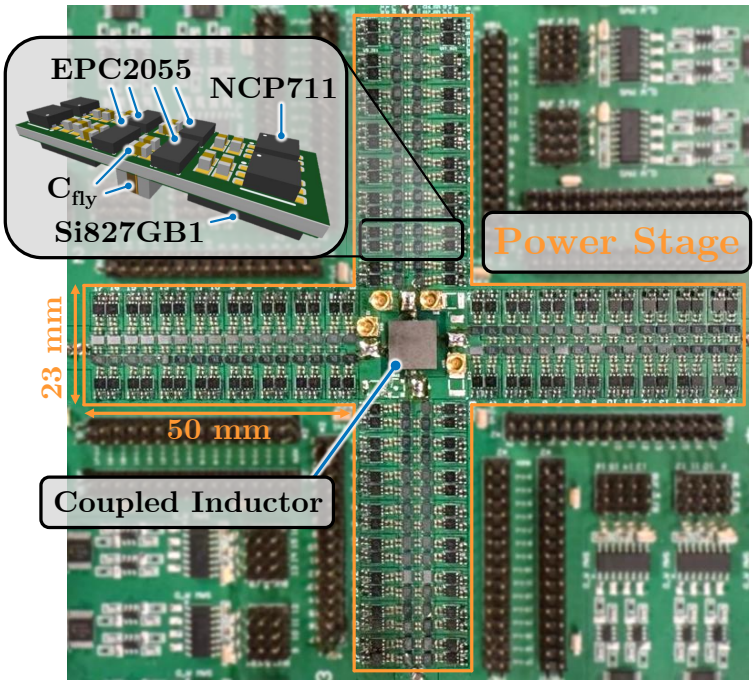


Figure 4.8: Four-phase, 17-level FCML converter with coupled inductors.

Table 4.1: Circuit Parameters of the FCML Prototype

f_{sw}	V_{dc}	C_{fly}	L_l	L_μ	C_o
500 kHz	48 V	10 μF	20.4 nH	230 nH	0.1 μF / 0.7 μF

4.3.3 Summary of Large-Signal Tracking Capabilities

The large-signal tracking capabilities of interleaved converters, as derived in the preceding sections, are summarized in Fig. 4.7. For this plot, we assume $N = 64$ as an example, and assume that the LPF cutoff frequency is set to one-eighth of the effective switching frequency. A buck converter has a tracking range limited below the cutoff frequency. On the other hand, a highly interleaved triangle-modulated converter can track-full amplitude signals up to $f_{\text{ref}} = \frac{2f_{\text{sw}}}{\pi}$, after which the slope of the reference must be kept below the carrier wave, leading to a -6 dB/dec maximum gain roll-off with frequency. The triangle modulator restricts the reference amplitude slightly under the ideal limit (4.6). In a practical design, the cutoff frequency of the interleaved converter may need to be set lower to filter sidebands depending on their frequency and magnitude.

The signal tracking range of the interleaved converter is larger than a buck converter and the harmonic performance is better in their overlapping range. Fig. 4.7 may be likened to the Bode plot of an operational amplifier. By limiting the gain of the interleaved converter, we can dramatically increase the frequency range. For example, if we restrict $\frac{A_{\text{ref}}}{V_{\text{dc}}} \leq \frac{1}{8}$, the system will ideally have flat gain up to $8f_{\text{sw}}$, $N = 64\times$ higher than a buck converter. This is useful in many high speed applications needing fast tracking but not over a large amplitude. For example, communication-over-power technology like Li-Fi and visible light communication require a large dc signal to power a load, plus a small high frequency component for communication. Interleaved converters are able to efficiently deliver the high power dc component, while also achieving high frequency reference-tracking performance.

4.4 Experimental Results

To verify the large-signal tracking properties of interleaved converters, we design a four-phase, 17-level FCML converter with $64\times$ interleaving and coupled inductors for ripple reduction and flying capacitor balancing. The power stage schematic is highlighted in Fig. 4.1, along with the physical design in Fig. 4.8 with key component values listed in Table 4.1.

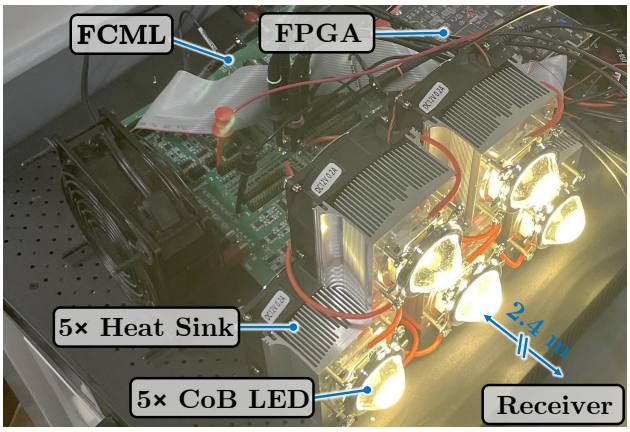


Figure 4.9: 400 W Li-Fi CoB LED transmitter array.

4.4.1 FCML Converter Design and Operation

Each FCML converter has 16 pairs of complimentary EPC2055 switches split into repeated switching cells with four switches and two half bridge drivers (Si827GB1-IS1) each. The switching cell, highlighted in Fig. 4.8, is designed with the low-inductance principles in [91] for maximum density and speed. There are 15 flying capacitors C_{fly} per phase with ideal dc voltages at evenly spaced fractions of the input voltage V_{dc}, starting at $\frac{15V_{\text{dc}}}{16}$ closest to the input and decreasing to $\frac{V_{\text{dc}}}{16}$ closest to the output. The flying capacitors are balanced by the coupled inductors at the output [72], which also serve to reduce the ripple and size of the magnetics. Each of the 64 gate signals are generated with phase shifted carriers according to eq. (4.1) and Fig. 4.10(a), where each complementary pair of switches is driven with an isolated half-bridge gate driver powered by a bootstrapping and regulation circuit [92]. The 64 open-loop gate signals are provided by an EP4CE15F23C8 FPGA operating with a 224 MHz internal clock to compare a digital counter and LUT to follow arbitrary reference signals. The steady-state operation at $d = 0.23$ is shown in Fig. 4.11 with good balancing provided by the coupled inductors. This plot does reveal one limit of large-scale interleaving: due to the differences in propagation delay (including from the PCB traces themselves), there is a phase shift variation of a few nanoseconds per phase, which means that the harmonic cancellation is not perfect; thus, the ripple is dominated by components below the effective switching frequency. Finally, Fig. 4.12 shows the converter tracking reference

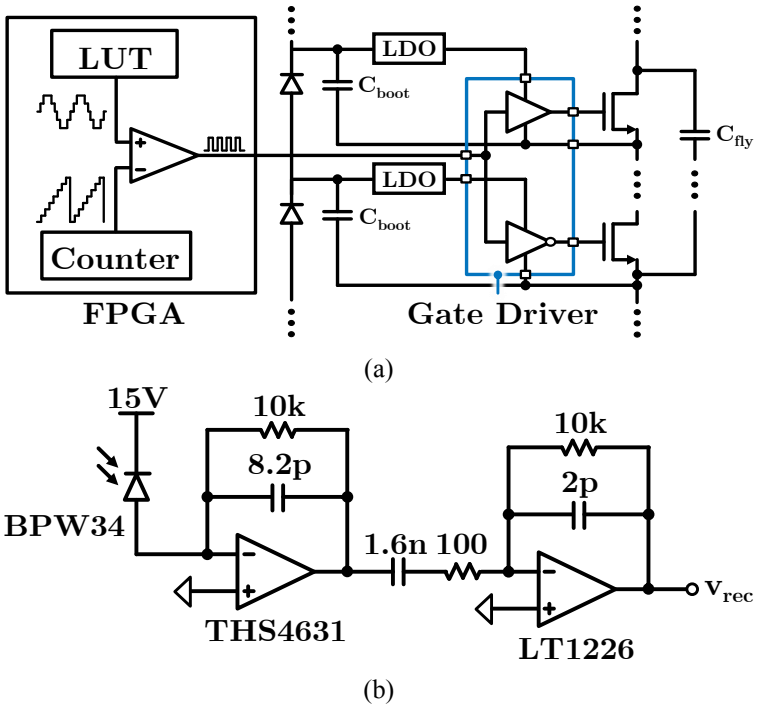


Figure 4.10: Schematic of the (a) FPGA signal generation and bootstrapping and (b) light receiver filtering and amplification circuit.

signals at points (a), (b), and (c) on Fig. 4.7. At low frequency, the converter tracks the signal with very high resolution due to the $64\times$ interleaving. Fig. 4.12(b) and (c) show the converter tracking with distortion outside of the allowable large-signal range with trailing- and double-edge modulation.

4.4.2 FCML Powered Li-Fi Transmitter Experimental Setup

The FCML converter is used to directly power an array of five Chanzon 100 W high-brightness CoB (chip-on-board) LEDs on heat sinks, as shown in Fig. 4.9. The LEDs have a forward voltage of around 31 V, so an average duty cycle of $d = \frac{31}{48} = 0.65$ is used, plus a data signal on a 1.2 MHz sinusoidal carrier, $2.4\times$ higher than f_{sw}. In accordance with the theory of section 4.3, the amplitude is limited to $A_{ref} < \frac{V_{dc}}{1.2\pi}$. Because of the high carrier frequency, the signal is imperceptible to the human eye. The LEDs are pointed at a light receiver circuit 2.4 meters away which amplifies and band-pass filters the communication signal (Fig. 4.10(b)).

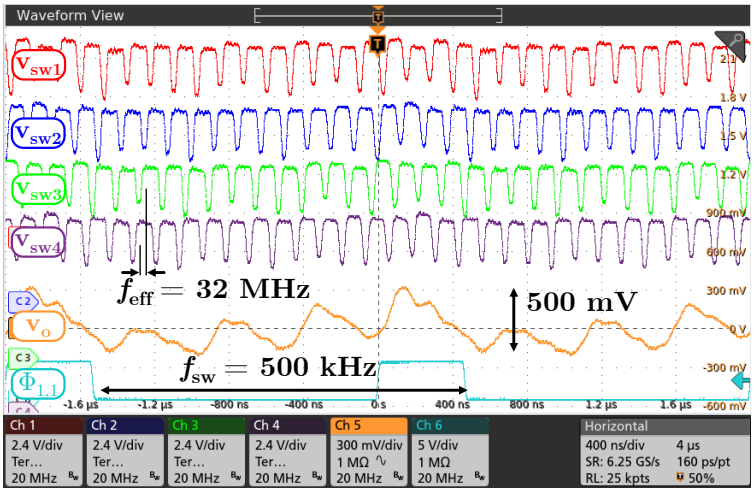


Figure 4.11: Steady-state switching waveforms of four switch nodes and output.

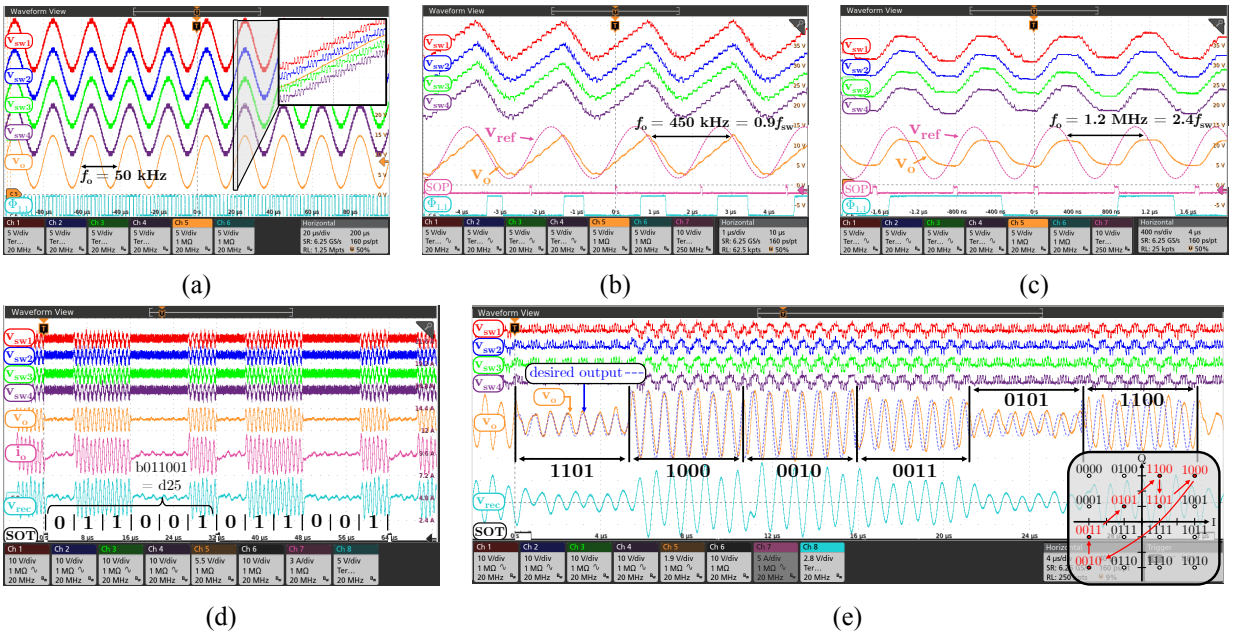


Figure 4.12: Converter operation (a) well below the switching frequency, beyond large-signal limits with (b) trailing- and (c) double-edge modulation, and Li-Fi LED transmission and reception modulated at 1.2 MHz with (d) OOK, sending “25” (APEC 2025), and (e) 6 symbols of 16-QAM.

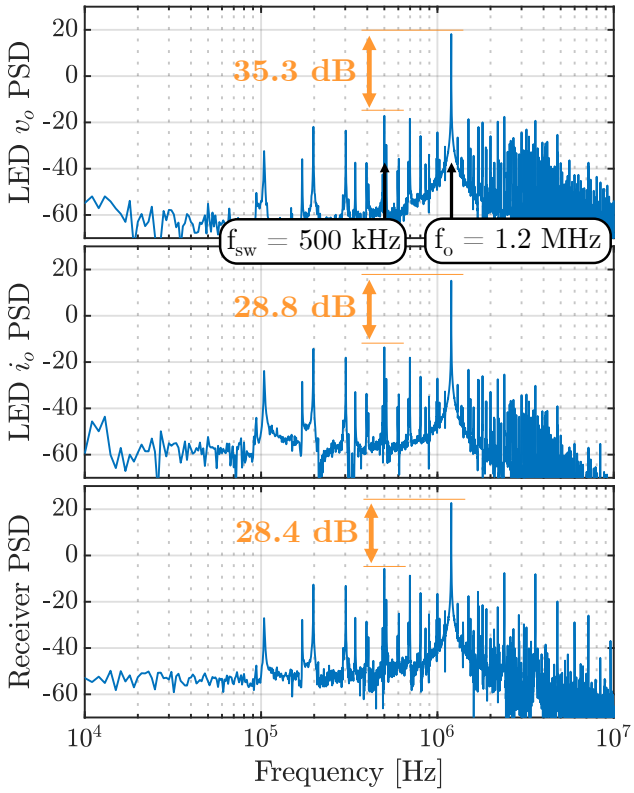


Figure 4.13: PSD of single-frequency sinusoid tracking at the LED voltage, current, and amplified photodiode output.

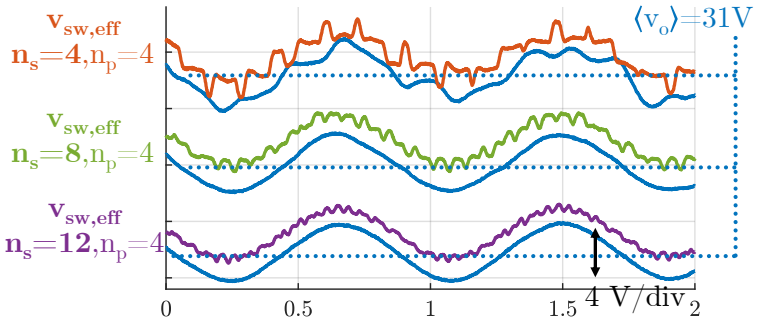


Figure 4.14: LED driving performance with 5, 9, and 13 levels, showing increasing resolution with increasing levels.

4.4.3 Visible Light Communication Performance

To minimize the impact of the timing mismatch ripple (section 4.4.1), the output capacitance is increased to $C_o = 0.7\ \mu$F, making $f_{LC} = 1.3$ MHz given the leakage inductance $L_l = 20.4$ nH of the inductor. With the output carrier frequency $f_{\text{ref}} = 2.4 f_{\text{sw}} = 1.2$ MHz, amplitude $A = \frac{V_{\text{dc}}}{9.2}$ (point (d) in Fig. 4.7), the PSD (power spectral density) of the LED voltage, current, and received voltage are shown in Fig. 4.13. The signal-to-noise ratio to the largest noise component at f_{sw} is high for all three, with some degradation due to the nonlinear LED I-V relationship which could be compensated with closed-loop control/pre-distortion. The output power is **383.4 W** and the conversion efficiency is **95.5%**, reduced negligibly from **96.0%** when no signal is transmitted. The gate drive loss and signal path loss are not included in the efficiency calculation. Fig. 4.12(d) and (e) shows the transmission of signals encoded with OOK (on-off keying) and 16-QAM. The converter output voltage faithfully reproduces the desired signals with a carrier frequency much higher than the switching frequency.

Practical problems remain with the optimization of interleaved converter design and with the experimental setup used here as an example. The problem of imperfect phase shifting sets a limit on the achievable harmonic cancellation. This, along with other non-idealities such as device packaging, layout space, and parasitics introduced by interleaving, may decide the optimal level of interleaving for a given application. Fig. 4.14 shows the LED reference signal tracking experiments repeated for the converter operated with 5-, 9-, and 13- levels, where increasing levels does improve resolution, but perhaps with an upper limit determined by practical factors. We have studied open-loop converters assuming good balancing and avoiding beat-frequency harmonics; the closed-loop behavior and stability around problematic frequency ratios, and the influence of coupled inductors are not studied here.

4.5 Chapter Summary

Multiphase interleaving, multilevel interleaving, and magnetic coupling multiply the effective switching frequency, reducing the required passives size and extending the signal tracking ca-

pabilities to and above the switching frequency of power electronics as long as the large-signal slope limits are not exceeded. This property is leveraged in an ultra-fast Li-Fi transmitter design using a 64× interleaved four-phase, 17-level FCML converter with coupled inductors for passive balancing. This enables above-switching-frequency small-signal Li-Fi communication on top of high efficiency power for a 400 W transmitter.

5

Applying the Multiplex Coupled Magnetics Power Architecture to Signal-over-Power Transmission

The contents of this chapter are from a manuscript currently in preparation: D. H. Zhou, M. Chen et al., (2025).

Abstract

Power electronic architectures combining multilevel switching, multiphase interleaving, and coupled magnetics provide scalable, intrinsically balanced frequency multiplication, enabling the use of small passives and fast modulation of the output without compromising efficiency by increasing the switching frequency. This makes them attractive in simultaneous signal-and-power delivery applications, where they can drive dual-use power electronics systems with both high efficiency and high data throughput; in particular, they can unlock long distance, high power, wide angle visible light communications that are critical for large-scale light fidelity applications. This chapter studies the theory of these scalable architectures and applies them to design a four-phase, seven-level multilevel converter passively balanced by coupled magnetics. The prototype achieves state-of-the-art signal-and-power delivery performance, providing 1000 W of wide-angle LED illumination at 95.8% efficiency while simultaneously transmitting data at 6.4 Mbps with a 8.033% error vector magnitude at a distance of 20 meters.

5.1 Chapter Introduction

As modern power infrastructure supports increasingly complex, numerous, and data-intensive smart devices, the need for power electronics that can transmit energy and information simultaneously is growing [14]. Power electronics leveraging ”talkative power” [93] can be used to transmit data and power together on dual-use power infrastructure, such as in the case of power-line communications [94], which enables effective coordination of distributed energy resources. Simultaneous signal-and-power transmission can also use wireless mediums; in particular, Li-Fi (light fidelity) is an emerging application where data is encoded in high-frequency modulations of LED brightness, providing illumination and secure communications that are invisible to both the human eye and radio frequency systems [77].

Li-Fi can unlock a broad communication spectrum leveraging existing, efficient LED lighting resources in homes, factories, hospitals, and other data-dense settings [95]. While extremely high

throughput have been achieved (e.g. [96]), highlighting the bandwidth potential of visible light communications (VLC), most demonstrations have been performed at low optical power (mW range) and short distances, or relying on long-distance beamforming and alignment that diminishes their illumination utility.

Talkative switched-mode power electronics offer a solution for efficiently driving wide-angle, high-power visible light communication systems [97–102]. However, current prototypes are still limited in their useful communication and illumination range and power level, especially given the moderate data rates. Increasing the data rate is typically accomplished increasing the switching frequency [12, 49, 78], but this also increases the switching loss, which in turn limits the power level and efficiency. Many current designs also require large power combiners, complex filters, and external LED biasing that reduce their practicality for driving space-constrained Li-Fi systems.

Multilevel switching [22, 57, 69, 103] and multiphase interleaving [19, 21, 26, 47] multiply the effective switching frequency of a converter, enabling faster output modulation [89, 104, 105] and smaller passives without needing to increase the switching frequency or switching loss. Multilevel hybrid switched-capacitor topologies, in particular, can deliver high power and high densities by using minimal inductor volume and many energy-dense capacitors [79, 80]. Multilevel converters, which traditionally suffer from voltage balancing challenges [34, 38, 43, 44, 46], can be balanced using coupled magnetics [72], including in dynamic contexts [106] and with very high level counts [107]. The passive balancing benefits of coupled magnetics are in addition to their well-known improvements to volume, bandwidth, and ripple [5, 27, 56, 84].

This article studies architectures that multilevel switching, multiphase interleaving, and coupled magnetics; when combined together, these techniques enable scalable, dense, balanced frequency-multiplied power electronics that can transmit high frequency data with low frequency switches. These principles are used to develop a passively balanced, four-phase, seven-level flying capacitor multilevel (FCML) converter that transmits data at multi-megahertz frequencies (6.4 Mbps) while efficiently (95.8%) converting power (1000 W) with only a 800 kHz switch-

Table 5.1: Comparing Converter Access Frequencies

Component or Signal	Single-Phase, Two-Level, Uncoupled Magnetics	Multiphase, Multilevel, Coupled Magnetics
switches	same frequency	lower frequency → lower switching loss
passives	same frequency	higher frequency → faster and smaller size
input signal sampling	same frequency	higher frequency → faster signal throughput

ing frequency. The architecture is passively balanced by a single four-phase coupled inductor, a method which is scalable, robust, and requires no active intervention. The entire system uses only a single 80 V input supply, no power combiner, and a new complementary switch bootstrapping technique being used to eliminate a separate gate driving supply and minimize losses. In an outdoor communication experiment, the prototype is used to drive 1000 W of wide-angle LED illumination while also transmitting 6.4 Mbps data modulated with 32-QAM (quadrature amplitude modulation) and 8.4% equalized RMS EVM (root-mean-squared error vector magnitude) at a distance of 20 meters.

The rest of this article is organized as follows. Section 5.2 overviews the principles of the multilevel, multiphase, coupled magnetics architecture, including passive voltage balancing, frequency multiplication, and above-switching-frequency communications. Section 5.3 applies these principles to design the four-phase, seven-level coupled inductor FCML prototype, including multilevel switching cells, inductor design, gate driving, control, and layout. The communication experiment and measured results are listed in section 5.4. Section 5.5 discusses possible design changes to further improve performance. Finally, section 5.6 concludes the article.

5.2 Principles of the Multilevel, Multiphase, Coupled Magnetics Architecture

Fig. 5.1 shows the principles of the multilevel, multiphase, coupled magnetics architecture converting a power input and signal input (data) into a signal-and-power output. A traditional converter not using these techniques accesses its switches, passives, and samples the input signal at the same frequency. If the frequency is increased to reduce the passive size or track faster input signals, the switching loss also increases, reducing efficiency. The fundamental benefit of the

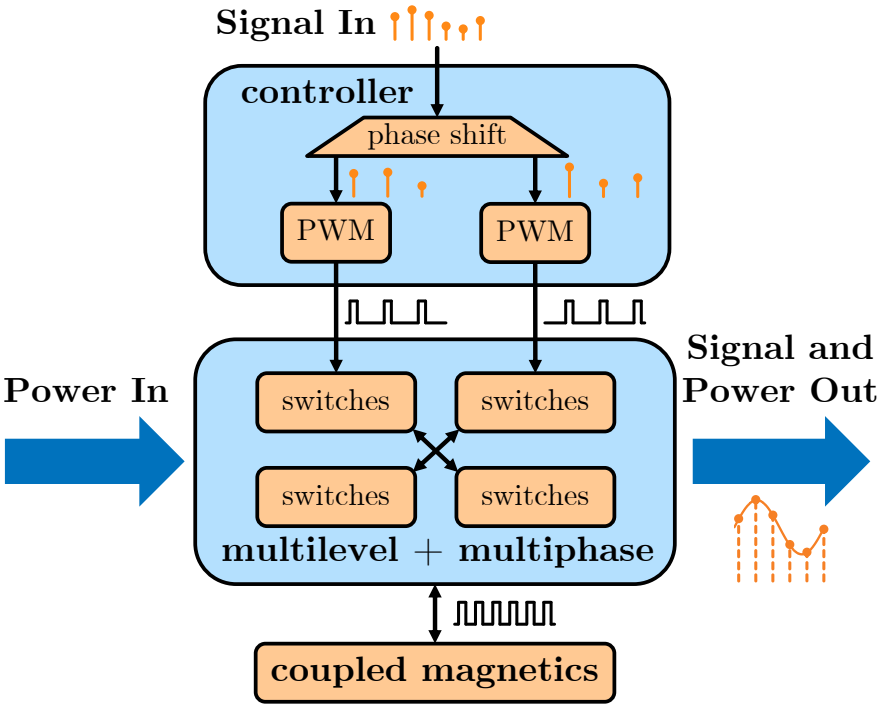


Figure 5.1: Block diagram illustrating the multilevel, multiphase, coupled magnetics architecture its application to signal-and-power loads.

architecture in Fig. 5.1 is a decoupling of the switching, passive, and sampling frequencies. Multiple phase-shifted switches arranged in multilevel and multiphase units are toggled at a lower frequency, while the input signal sampling and passive access occurs at a higher frequency. This allows the converter to use smaller, faster passive devices and modulate higher frequency and higher throughput signals without needing to increase the switching frequency or switching loss. Table 5.1 summarizes these fundamental architectural differences.

Fig. 5.2(a) shows an implementation of the multilevel, multiphase, coupled magnetics architecture consisting of $M\times$ FCML (flying capacitor multilevel) units combined by an M-phase coupled inductor. Each multilevel unit consists of K switched capacitor (SC) cells, for a total of $2\times M\times K$ switches and $M\times K-M$ flying capacitors, with the SC units closest to the input using the input capacitors.

The switching waveforms are shown in Fig. 5.2(b). The K switches in each multilevel unit are evenly time shifted by $\frac{T_{sw}}{K}$ (where $T_{sw} = \frac{1}{f_{sw}}$ is the switching period and f_{sw} is the switching frequency) to that the M switch nodes have evenly spaced pulses; then, the $M\times$ multilevel units

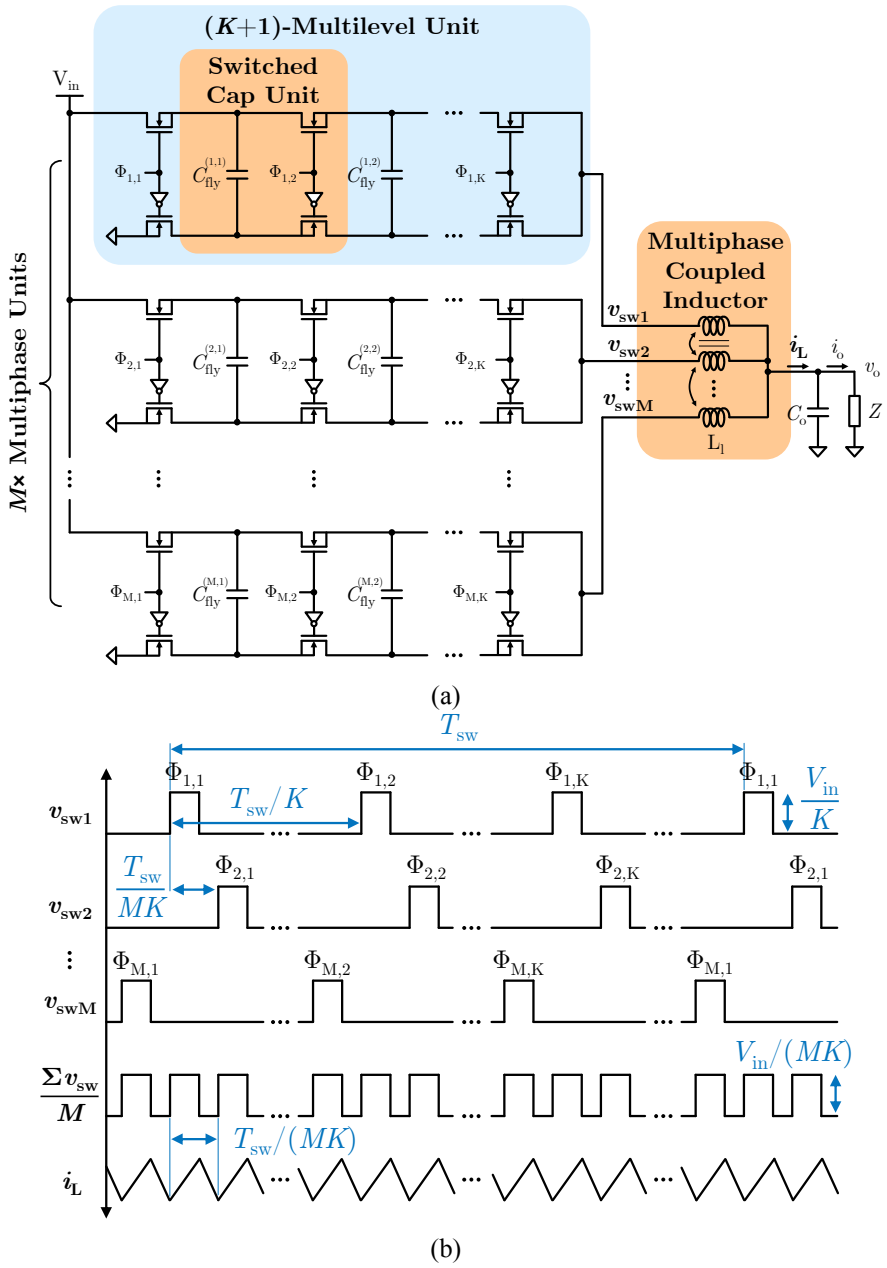


Figure 5.2: (a) Implementation of the multilevel, multiphase, coupled magnetics architecture with $M \times K + 1$-level FCML units, and (b) switching waveforms of the illustrated structure.

are themselves time shifted by $\frac{T_{sw}}{MK}$ so that the combined switch nodes form a uniform pulse train with an effective multiplied frequency $f_{eff} = M \times K \times f_{sw}$. The output current i_L ripples at this multiplied frequency, reducing the required passive component size.

5.2.1 Passive Voltage Balancing using Coupled Magnetics

The use of coupled inductors is essential for balancing the multilevel units, and thus to the scalability of the architecture. Ideally, the flying capacitors voltages are balanced at

$$C_{fly}^{(m,k)} = V_{in} \times \frac{K-i}{K} \tag{5.1}$$

for $m = 1, \ldots, M$ and $i = 1, \ldots, K-1$. When balanced, adjacent flying capacitors clamp the blocking voltage of the switched capacitor cells to

$$V_{blk} = \frac{V_{in}}{K}. \tag{5.2}$$

Balancing the flying capacitors will balance the input voltage stress evenly across the K SC units. As the switching frequency, number of SC units, and number of flying capacitors increases, it becomes more difficult to balance them [34]. Therefore, the scalability and practicality of the architecture depends on the passive voltage balancing provided by coupling the inductors proven in [72]. If the inductors are coupled, a voltage imbalance on one multilevel unit will couple to the other phases, generating a small opposing imbalance that reduces the initial disturbance, thus forming a negative feedback balancing loop. This property applies to converters with any number of levels and any even number of phases, with some singularities that are managed by tightly coupling the inductors and allowing some asymmetry in the system.

Fig, 5.2 shows the coupled inductor being implemented as a M-phase device, which minimizes per-phase ripple and magnetic volume [26], but it can also be implemented as several coupled inductors with fewer than M phases, so long as each is even-numbered.

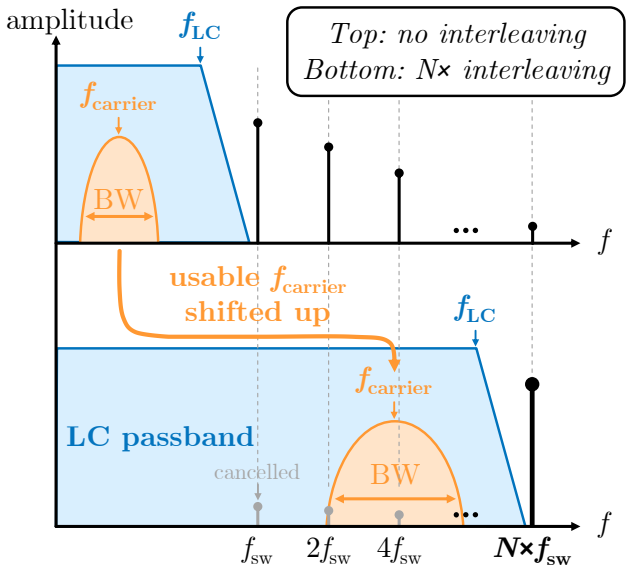


Figure 5.3: Frequency plot of switching harmonics and communication bandwidth of the proposed architecture. The *LC* filter is designed to filter the undesired switching harmonics starting at the effective switching frequency, while passing the desired communication signal. The lower frequency switching harmonics are canceled by interleaving the switches.

5.2.2 Output Signal Modulation Beyond the Switching Frequency

Traditionally, the maximum modulation frequency of a converter is well below the switching frequency because of the Nyquist sampling theorem [89] and attenuation from the LC filter [19]. By balancing and scaling up the multiphase, multilevel, and coupled inductor units, we can use the architecture to track signals up to and even above the switching frequency. Above-switching-frequency signal modulation is achieved in three steps.

1. By generating an independent PWM signal for each switch, the effective sampling frequency is multiplied by $M \times K$, theoretically multiplying the frequency of signals that can be reconstructed by the converter (in the sense of Nyquist) by $M \times K$ also [105].

2. The lower frequency switching harmonics at f_{sw}, $2f_{sw}$, up until (but not including) $f_{eff} = M \times K \times f_{sw}$ are canceled as shown in Fig. 5.3, assuming the converter is well balanced (by coupled inductors) and well timed. This means the LC filter cutoff frequency can be shifted from below f_{sw} to being above it, as the switching harmonics remaining in the passband are already canceled.

3. The coupled inductors, in addition to balancing the large-scale multilevel structure that enables 1) and 2), presents a low inductance during transient operation and a high inductance during steady-staet operation [26]. Parameterized in terms of the leakage inductance L_l and magnetizing inductance L_μ, it has been shown that the steady-state ripple is dominated by the magnetizing component and the transient behavior is dominated by the leakage component. Tightly coupled inductors with a high ratio $\beta = \frac{L_\mu}{L_l}$ thus enable the design of a high bandwidth LC output filter passing high frequency output signals while also sufficiently filtering the steady-state ripple. The LC resonant frequency of the output filter shown in Fig. 5.2 is [5]

$$f_{LC} = \frac{1}{2\pi\sqrt{C_o \frac{L_l}{M}}}. \tag{5.3}$$

Fig. 5.3 illustrates the sampling frequency multiplication, harmonic cancellation, and LC filter frequency extension that enable signal output (e.g. on a carrier f_{carrier} with surrounding bandwidth) above the switching frequency f_{sw}. As shown in [104], when tracking signals above the switching frequency, their peak-to-peak amplitude must be limited to avoid distortion. Assuming the PWM signals are modulated with a triangle wave carrier, the converter can track a sinusoid with frequency f_o and a ratio of peak-to-peak amplitude Δv_o to the input voltage, V_{in} as large as

$$\frac{\Delta v_o}{V_{\text{in}}} \leq \frac{2f_{\text{sw}}}{\pi f_o} \tag{5.4}$$

without distortion. The capability of the multiphase, multilevel, and coupled magnetics structure to operate at lower switching frequencies but modulate high frequency, low amplitude signals is extremely useful for simultaneous communication and power delivery applications. With just a simple coupled inductor filter, the multiphase and multilevel units can synthesize arbitrary high frequency waveforms, including advanced modulation schemes with pulse shaping and digital pre-distortion.

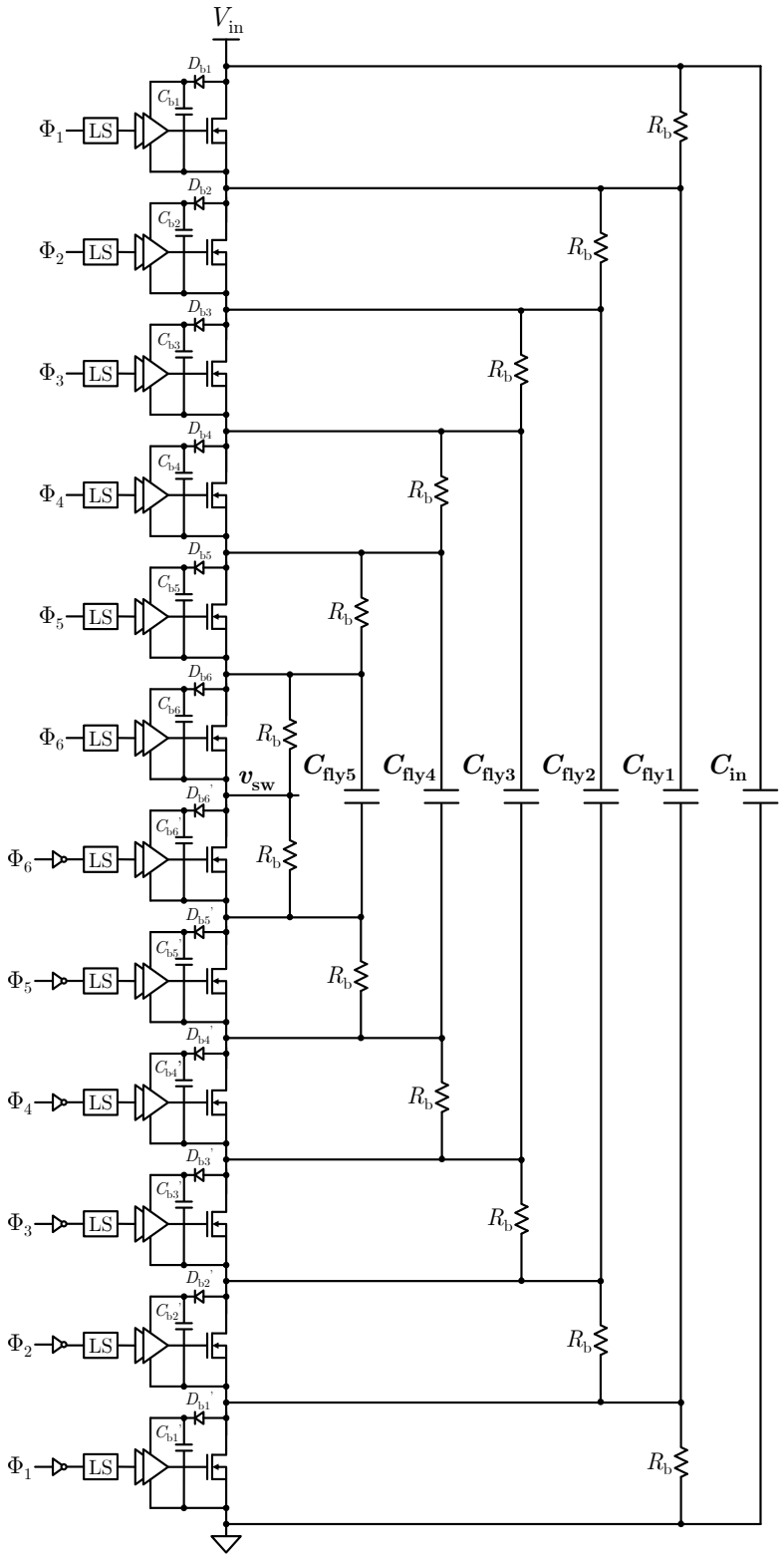


Figure 5.4: Schematic of one seven-level FCML unit consisting of six complementary switch pairs driven by floating gate drivers, bootstrap supplies, and five flying capacitors.

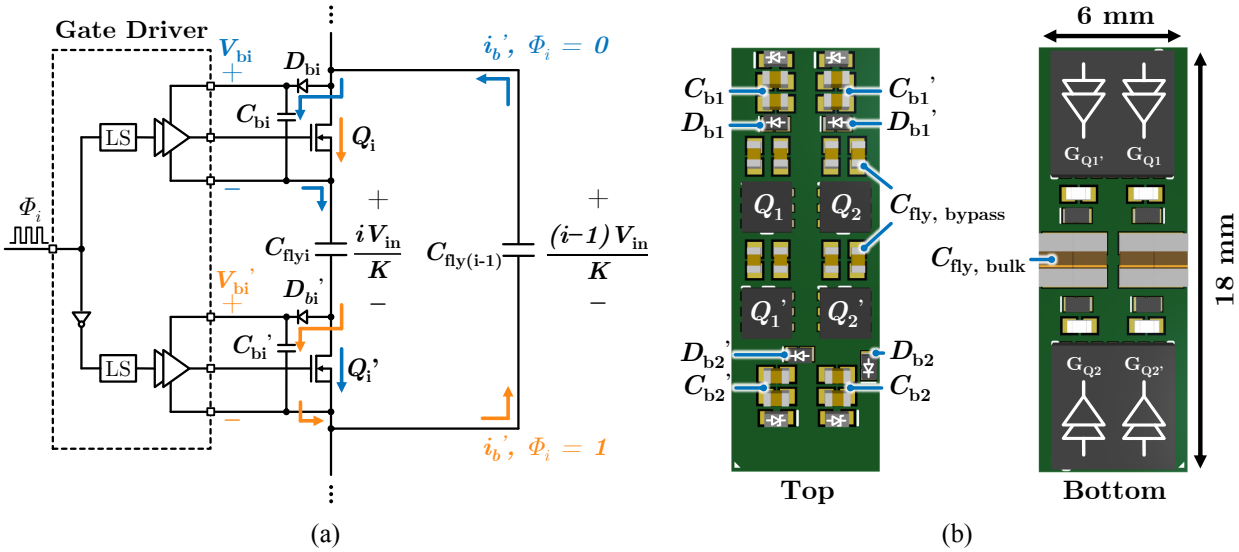


Figure 5.5: (a) Schematic of the switched-capacitor cell repeated six times for each multilevel unit. The bootstrap capacitors of each switch are charged by the adjacent flying capacitors when their complementary switch is on. (b) Layout of two of the repeatable switching cells.

5.3 Design of the 24× Interleaved FCML Signal-and-Power VLC Transmitter

The use of many repeatable, scalable multilevel switched-capacitor cells, passively balanced by coupled inductors, is essential to achieve high modulation frequency and communication throughput with moderate per-switch frequencies. This section details the design of an 80 V input, four-phase, seven-level FCML converter with a four-phase coupled inductor.

5.3.1 Multilevel Unit Design

The input voltage of 80 V, selected to allow step-down driving of a medium-voltage string of series-connected LEDs, is regulated by the six series-stacked switches of the seven-level units shown in Fig. 5.4. The switch blocking voltages are clamped by the adjacent flying capacitors to $\frac{V_{in}}{6} = 13.\overline{3}$ V. This allows the use of 20 V switches for good device utilization with a sufficient safety margin.

Most of the multilevel switches are not ground referenced and require floating gate drivers and gate drive supplies. Most methods for generating the floating gate drive supplies involve a separate bootstrapping input supply and several auxiliary components (e.g. LDOs, charge pumps) [92]. Therefore, these methods can incur significant loss from large LDO step-down ratios for

the lowermost switches (closer to ground), and from cascaded diode drops for the uppermost switches (closer to V_{in}).

To address these limitations, the floating gate supplies for the multilevel units are generated with a single bootstrap diode and capacitor for each switch, as shown in the closeup of one complementary pair in Fig. 5.5(a). Although the complementary switches are not necessarily connected from drain-to-source, the blocking voltage of each switch (when its complement is on) is always clamped by the flying capacitors (if balanced) to $\frac{V_{\text{in}}}{K}$. When off, this voltage source is used to charge a source-referenced bootstrap capacitor (C_{bi} and C'_{bi} in Fig. 5.5(a)), providing a voltage

$$V_{\text{bi}} = V'_{\text{bi}} = \frac{V_{\text{in}}}{K} - V_{\text{D}} \tag{5.5}$$

for gate driving, where V_{D} is the diode drop. When $i = K$, the inner flying capacitor in Fig. 5.5(a) is simply a short, and the bootstrapping technique reduces to the the standard bootstrapping technique for a high-side NMOS buck converter [19]. When $i = 1$, the outer flying capacitor is simply the input capacitor.

As annotated in Fig. 5.5(a), the charge that charges both bootstrap capacitors in a complementary pair comes from the higher voltage flying capacitor. This technique relies on the flying capacitors being balanced, including from the charge being taken to charge the bootstrap supplies, which is accomplished by the coupled inductors.

If the switch $V_{\text{gs,max}} \geq V_{\text{ds,max}}$, the bootstrap capacitor voltage (5.5) can be directly used for gate drive, which maximizes the drive voltage and minimizes the on-resistance. If the switch $V_{\text{gs,max}} < V_{\text{ds,max}}$, an LDO may be used to step down the voltage.

The converter cannot start switching until the bootstrap voltages exceed the gate driver UVLO, and the coupled inductors do not balance the flying capacitors before switching begins. Therefore, the multilevel unit in Fig. 5.4 implements a resistor balancing network (RBN) that precharges the flying capacitors prior to switching [41]. The resistors can be very large and consume a negligible amount of power since the coupled inductors take over balancing responsibilities after switching begins. The converter can begin switching after the input voltage rises enough

enough for the bootstrap voltages to exceed exceed the gate driver UVLO V_{UVLO}

$$V_{\text{bi}} = V'_{\text{bi}} = \frac{V_{\text{in, rising}}}{2K} - V_{\text{D}} > V_{\text{UVLO}}$$
$$\rightarrow V_{\text{in, rising}} > 2K(V_{\text{UVLO}} + V_{\text{D}}) \tag{5.6}$$

for all $i = 1, 2, \ldots, K$. The startup procedure has built in hysteresis, because the bootstrap voltages, which initially charge to $\frac{V_{\text{in}}}{2K} - V_{\text{D}}$, charge to $\frac{V_{\text{in}}}{K} - V_{\text{D}}$ when their complementary switch turns on. Therefore, after switching has begun, it can continue as long as the input voltage remains above

$$V_{\text{in}} > K(V_{\text{UVLO}} + V_{\text{D}}). \tag{5.7}$$

Fig. 5.5(b) shows the layout of a two of the repeatable switching cells drawn in Fig. 5.5(a). The layout pairs the switching cells because of the differing device widths of the chosen switches (Vishay SIA466EDJ) and gate drivers (Skyworks Si8234AB-D). The flying capacitors are implemented with 0402 0.1 μF bypass capacitors on the top layer that minimize the high frequency switching loop, plus 0805 2.2 μF bulk capacitors on the bottom layer that provide dense energy storage. All capacitors are 100 V rated. The floating gate drivers are implemented on the bottom layer to minimize the gate driving loop size, and are powered by the bootstrapping diode and capacitors on the top layer. The layout also shows Zener diodes in parallel with the bootstrap capacitors which protect the gate drivers from over-voltage.

5.3.2 Multiphase Coupled Inductor Design

The coupled inductor is designed for tight coupling to minimize ripple and maximize passive balancing strength, along with a low leakage inductance for a high LC filter frequency allowing high frequency modulation of the output. To meet these goals, a custom four-phase PCB-embedded coupled inductor core with dimensions 9 × 9 × 5 mm is designed using DMEGC DMR53 material, as shown in Fig. 5.6. The windings are implemented with two PCB windings per phase, overlapped and interleaved to minimize the magnetization of the core, proximity effect, and

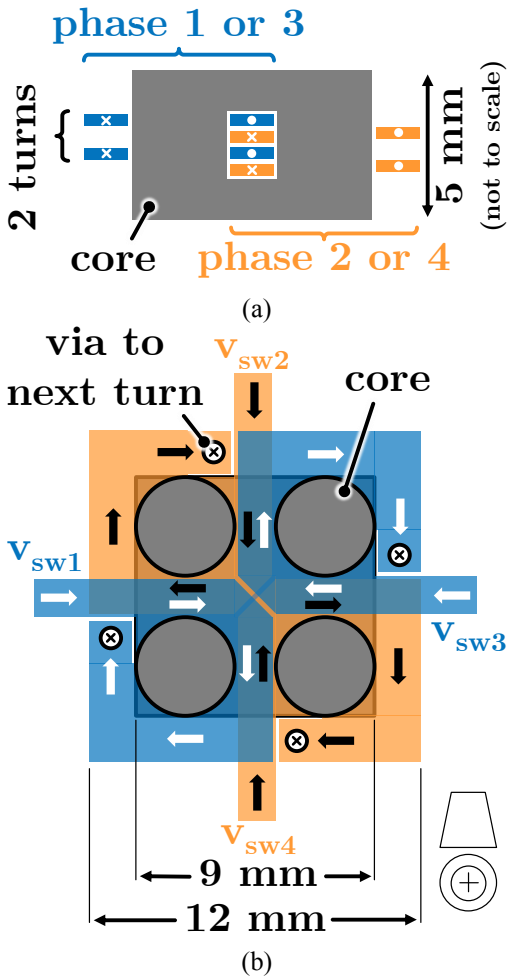


Figure 5.6: (a) Side and (b) top view of the coupled inductor with PCB windings.

Table 5.2: Operating Parameters of the FCML Prototype

Symbol	Parameter	Value
V_{in}	Input Voltage	80 V
V_{out}	Average Output Voltage	37 V
f_{sw}	Per-Switch Switching Frequency	800 kHz
f_{eff}	Effective Switching Frequency	19.2 MHz
f_{LC}	LC Filter Resonant Frequency	6.2 MHz
f_{carrier}	Signal Carrier Frequency	3.84 MHz
L_l	Leakage Inductance	13.2 nH
L_μ	Magnetizing Inductance	109 nH
L_μ/L_l	Coupling Ratio	8.26
C_o	Output Capacitance	0.2 μF

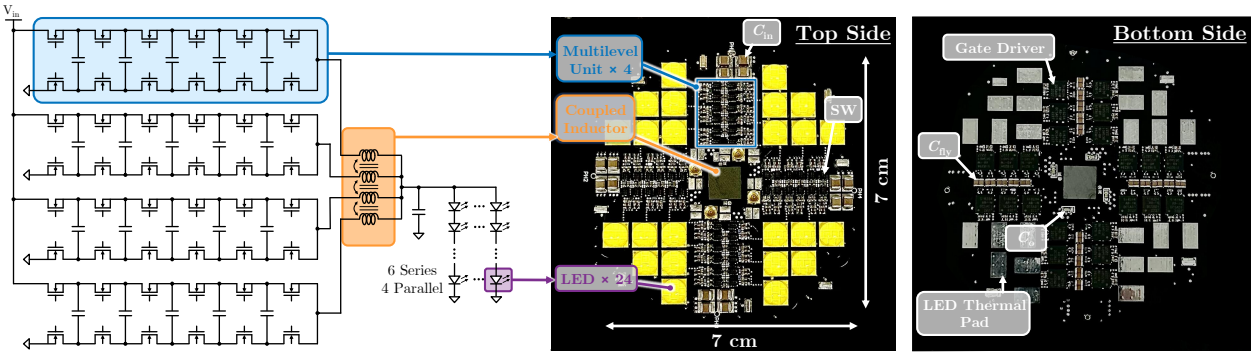


Figure 5.7: Complete multiphase, multilevel, coupled magnetics VLC transmitter featuring four multilevel units, four-phase coupled inductors, and 24 on-board LEDs. The heat sinks (not shown) are attached to the exposed bottom-side thermal pads for the high power experiments.

winding resistance [108, 109].

The coupled inductor achieves a leakage inductance of $L_l = 13.2$ nH and a coupling ratio of $\frac{L_\mu}{L_l} = 8.26$. The low leakage inductance allows a high LC filter frequency with a reasonable output capacitor size, and the high coupling ratio reduces the current ripple and multilevel voltage imbalance. The complete output filter parameters are listed in Table 5.2 along with the relation between the filter frequency, switching frequency, and effective multiplied frequencies. The switching frequency is set at 800 kHz, which balances efficiency and output frequency, as further verified in section 5.4.

5.3.3 Load, Control, and Communication Design

Cree XFL05K-6V are chosen for the LEDs for their high power rating and dense surface mount package which allows them to be soldered on-board with the converter. A total of 24 LEDs are used, split into four parallel strings of six series LEDs. At the targeted LED forward voltage (6.1 to 6.25 V), this implies an average output voltage of approximately 37 V. This selection ensures a duty cycle of approximately 50%, which balances the current stress between the high-side and low-side switches. The LEDs each have a t-Global TGH-0075-01 heat sink attached via thermal tape on an exposed pad on the back side of the board.

The converter is controlled by an EP4CE15F23C8 FPGA. To improve the PWM resolution, the FPGA clock frequency is maximized (326.2 MHz, 408 FPGA clock cycles per switching period), and the 24 phase-shifted PWM signals are drawn from a pre-generated look-up table. For the communication experiments, the PWM signals are modulated with a triangle wave carrier at a 46.25% average duty cycle and a 3.84 MHz carrier frequency. The carrier frequency is selected as high as possible, to maximize communication throughput, while still keeping the signal bandwidth in the LC filter passband, as illustrated in Fig. 5.3. Since the carrier frequency is 4.8× higher than the switching frequency, the maximum amplitude of the output signal is limited, by equation (5.4), to

$$\left.\frac{\Delta v_o}{V_{\text{in}}}\right|_{\text{max}} = \frac{2f_{\text{sw}}}{\pi f_o} = 0.132. \tag{5.8}$$

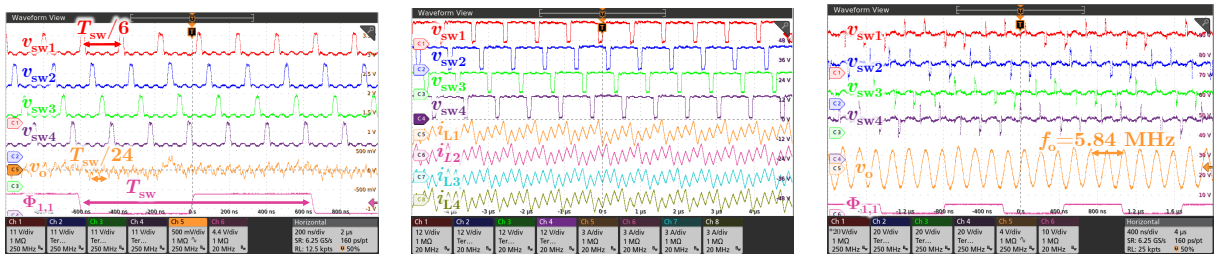
The peak-to-peak amplitude of the modulated signal is limited to the value in (5.8) to avoid distortion. The arbitrary modulation capability of the converter is leveraged to improve throughput and reduce receiver distortion by using QAM (quadrature amplitude modulation) and RRC (root-raised-cosine) pulse shaping.

5.4 Experimental Results

The full schematic and layout of the transmitter are shown in Fig. 5.7 and the important operating parameters and components are listed in Table 5.2 and Table 5.3 respectively. With the afore-

Table 5.3: Key Components of the FCML Prototype

Purpose	Component
Switches	48× Vishay SiA466EDJ (20 V)
Gate Drivers	24× Skyworks Si8234AB-D-IM
Flying Capacitors (bulk)	40× TDK 2.2 μF, 0805, X7R, 100 V
Flying Capacitors (bypass)	80× Murata 0.1 μF, 0402, X5R, 100 V
Bootstrap Diodes	48× onsemi NSR05F40NXT5G
Bootstrap Capacitors	48× Murata 2.2 μF + 0.1 μF, 0402, 25 V
Output Capacitors	2× Murata 0.1 μF, 0402, X5R, 100 V
LEDs	24× XFL05K-6V
Controller	EP4CE15F23C8



(a) (b) (c)

Figure 5.8: Converter operation with (a) duty cycle fixed at 52% and (b) 14.5%, showing the frequency multiplication of the switching frequency, FCML frequency, current ripple frequency, and effective switching frequency at the output. (c) The output voltage is then modulated to synthesize a 5.84 MHz sine wave, 7.3× higher than the 800 kHz switching frequency, centered at a 50% duty cycle and driving a 16 A electronic load.

mentioned 80 V input voltage, the converter begins switching, according to eq. (5.6), when V_{in} exceeds approximately 64 V. The total layout area, including input capacitors and the LEDs, is 49 cm^2, and the total power stage area, including gate drive but not input capacitors, is approximately 17 cm^2.

The basic operating conditions of the multiphase, multilevel, coupled magnetics converter are shown in Fig. 5.8. In Fig. 5.8(a), the four switch nodes of the multilevel units have a frequency of 4.8 MHz, six times higher than the switching frequency. The coupled inductors then combine the multilevel units, which are evenly phase shifted from one another, to produce an effective ripple frequency of 19.2 MHz at the output, 24× higher than the switching frequency. The switch node pulses are all at consistent levels, indicating the multilevel voltages are well-balanced by the coupled inductors. This balancing, along with good timing precision, means that the subharmonic ripples (at f_{sw}, $2 \times f_{\text{sw}}$, etc.) are successfully canceled.

Fig. 5.8(b) shows the inductor current ripples with the converter switching at $f_{\text{sw}} = 200$ kHz. The waveform shapes indicate the inductors are tightly coupled, multiplying the current ripple frequency to $24 \times f_{\text{sw}}$ and reducing the ripple amplitude. The inductor currents are measured with small wire loops and current probes, which decreases the coupling seen in Fig. 5.8(b) compared to the true coupling level as measured in Table 5.2.

Fig. 5.8(c) shows the converter output modulated with a 5.84 MHz sinusoid, $7.3\times$ higher than the switching frequency of 800 kHz, with a peak-to-peak amplitude ratio of approximately $\frac{\Delta v_o}{V_{\text{in}}} \approx 0.1$, respecting the amplitude limit calculated in eq. (5.8). This verifies that the converter can synthesize waveforms with frequency much higher than the switching frequencies.

The converter efficiency including gate drive losses is measured in Fig. 5.9 with a BK Precision 9115B power supply providing the $V_{\text{in}} = 80$ V, TTi LD400P electronic loads in parallel providing the $0 - 1000$ W constant current load, and the input/output voltages being measured with Keithley 179A multimeters. The peak efficiencies are $\{95.8, 97.3, 97.7\}$% and the full-load efficiencies are $\{95.6, 96.9, 97.3\}$% respectively for the three switching frequencies $\{200, 400, 800\}$ kHz. A switching frequency of 800 kHz is chosen for the communication ex-

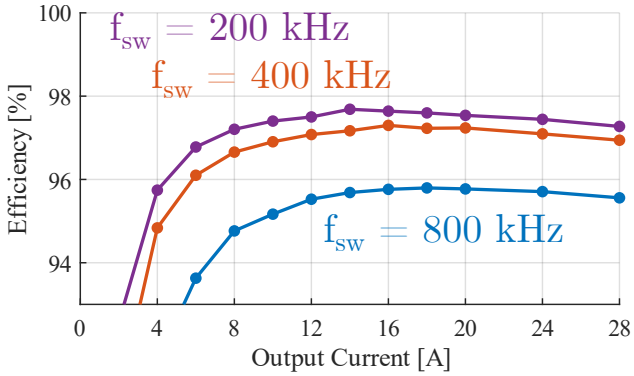
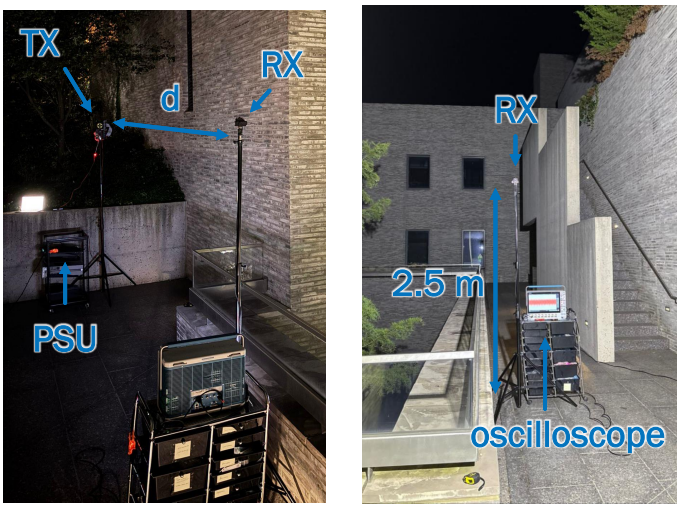


Figure 5.9: Converter efficiency across full load range with 50% duty cycle at $f_{sw} = 200, 400, 800$ kHz. The peak efficiency is between 95.8% and 97.7% depending on the switching frequency.



(a) (b)

Figure 5.10: Experimental setup of the outdoor VLC system. The transmitter and receiver (PDA10A) are elevated 2.5 m above the ground and placed a distance d=5-20 m from each other (5 m shown). The experiments are performed at night, clearly contrasting the illumination with the LEDs (a) off and (b) on.

periments, which trades off the the optimal efficiency for higher throughput.

5.4.1 Communication Experiment Setup

The communication experiments are performed outdoors at night near the Andlinger Center for Energy and the Environment in Princeton, New Jersey, as shown in Fig. 5.10. This setup simulates a real-world high-power outdoor illumination scenario similar to a stadium, arena, or stage, with various obstructions, secondary light sources, and surface materials experiment. The transmitter and receiver are elevated 2.5 meters above the floor and are positioned facing each other separated by a distance d between 1 and 20 meters. In the photo, d=5 m is shown.

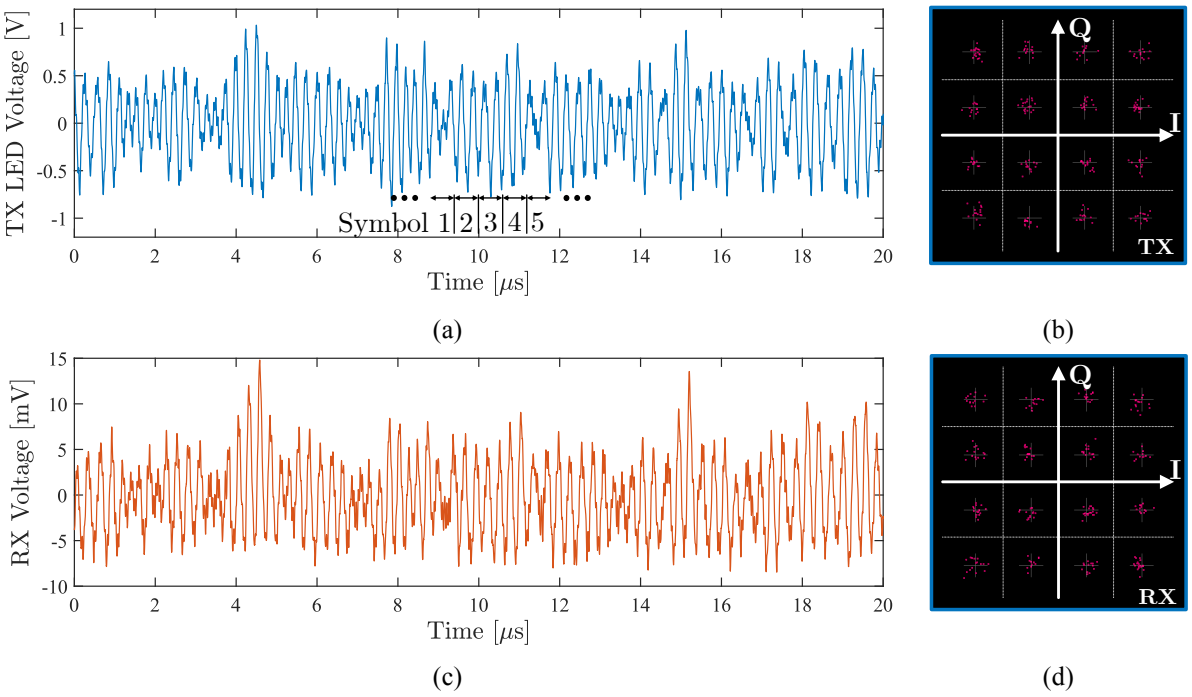


Figure 5.11: (a) Transmitted signal measured at the LED voltage and (b) associated constellation, (c) received signal measured at the detector output and (d) associated constellation.

Throughout the communication experiments, the data is modulated with a 3.84 MHz carrier frequency (4.8× higher than the switching frequency of 800 kHz), with a symbol rate of $R_s = 1.28$ Msymbol/s, one third of the carrier frequency. The signals are shaped with an RRC filter with $\alpha = 0.35$.

The receiver is implemented with a Thorlabs PDA10A photodetector. In some experiments (when noted), a Thorlabs SM1AD18 lens is fitted on the receiver. All transmitted and received signals are measured with a Tektronix MSO58 oscilloscope, and the communication signals are demodulated with the Tektronix SignalVu software. The received communications are equalized with the SignalVu software, while the transmitted signals (measured as the LED voltage) are not equalized.

Fig. 5.11 shows the transmitted and received signals at a distance of 1 m with low power (50 W output), low peak-to-peak amplitude ($\frac{\Delta v_o}{V_{\text{in}}} = 0.05$, no receiver lens, and 16-QAM modulation. A short distance is chosen for this illustrative example so that synchronized transmit and received signals can be measured simultaneously; in the proceeding subsections, only the

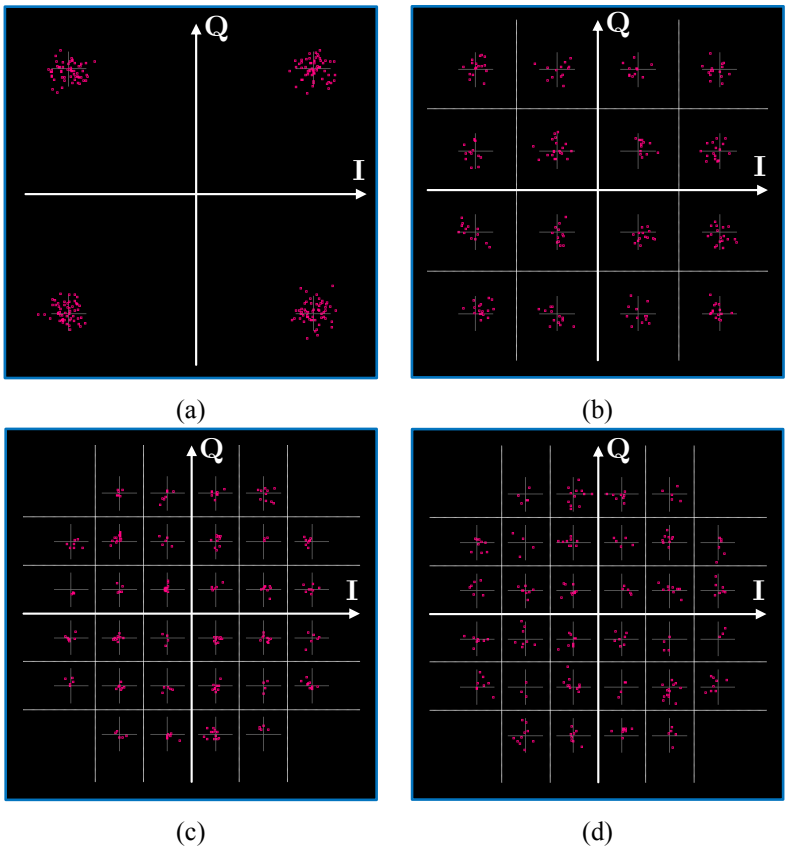
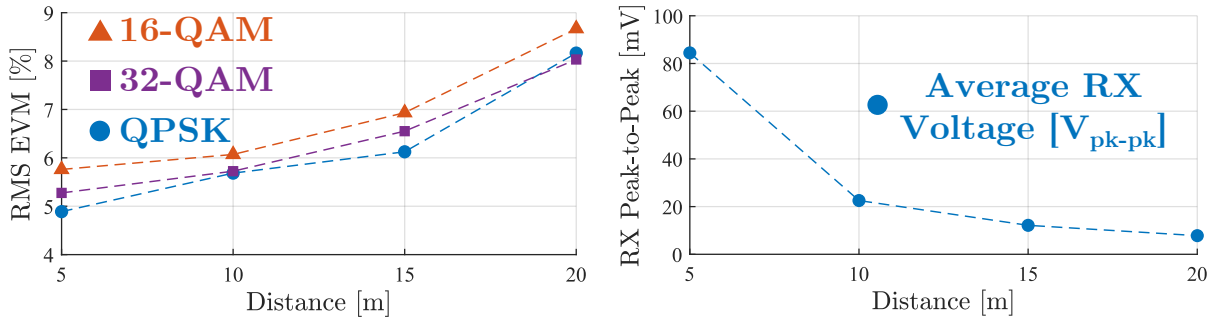


Figure 5.12: Constellations of demodulated and equalized receiver signals at a symbol rate of 1.28 MSymbols/s for (a) QPSK at 20 m, (b) 16-QAM at 20 m, (c) 32-QAM at 5 m, and (d) 32-QAM at 20 m.

received signals are measured. The 16-QAM constellations shown in Fig. 5.11 result after demodulation with the SignalVu software and correspond to a RMS/peak EVM of 7.682%/18.752% for the transmitter (not equalized) and 8.013%/20.951% for the receiver (equalized).

Table 5.4: Outdoor VLC Communication Performance at Receiver (Equalized)

Distance [m]	**RMS EVM [%]**			**Peak EVM [%]**			**RX Voltage, Peak-to-Peak [V]**		
	QPSK	16-QAM	32-QAM	QPSK	16-QAM	32-QAM	QPSK	16-QAM	32-QAM
5	4.888	5.760	5.275	10.285	12.050	12.832	84.57	85.95	82.81
10	5.684	6.070	5.724	12.940	12.616	14.469	22.18	23.24	22.21
15	6.125	6.933	6.551	14.347	16.339	15.715	12.09	12.43	11.93
20	8.165	8.670	8.033	19.508	18.334	19.759	7.973	7.785	7.696



(a) (b)

Figure 5.13: (a) RMS EVM as a function of distance between the transmitter and receiver and modulation scheme. The increase in EVM is clearly related to the quadratic decay in received power in (b), which approaches the noise level of the detector above 20 m.

5.4.2 Outdoor Communication Performance

The transmitter is used to drive the LEDs with an average duty cycle of 46.25% with a QPSK, 16-QAM, or 32-QAM signal modulated with a peak-to-peak output voltage of 10 V, corresponding to an average output power of 1000 W. The output amplitude to input voltage ratio is $\frac{\Delta v_o}{V_{\text{in}}} = 0.125$, which is less than the limit set by eq. (5.8) for the switching frequency to output frequency ratio.

Table 5.4 lists the RMS EVM, peak EVM, and peak-to-peak received voltage as measured by the PDA10A detector with a SM1AD18 lens attached. The EVM values are calculated from the demodulated SignalVu constellations, four examples of which are shown in Fig. 5.12. Since the symbol rate is fixed at $R_s = 1.28$ Msymbol/s, the bit rates of the three modulation schemes are 2.56 Mbps for QPSK, 5.12 Mbps for 16-QAM, and 6.4 Mbps for 32-QAM.

The increase in EVM with distance is primarily due to the inverse-squared reduction in received power. Since the design targets large-area illumination and wide communication access, the transmit power is spread over a large area by the wide-angle LEDs. Fig. 5.13 shows the RMS EVM plotted against distance, along with the average peak-to-peak receiver voltage. Beyond 20 m, the received signal approaches the sensitivity of the receiver and the signal can no longer be demodulated properly. The range can be extended by increasing the peak-to-peak signal amplitude, though this necessitates a reduction in the carrier frequency and throughput.

Table 5.5: Performance Comparison of the Multiphase, Multilevel, Coupled Magnetics VLC Transmitter to Other Designs

Ref.	Year	Note	Output Power [W]	Distance [m]	Bit Rate [Mbps]	RMS EVM [%]	Switching Freq. [MHz]	Peak Eff. [%]
This Work	2025	Multiphase 24× FCML, QAM	1000	20	6.4	8.03	0.8	95.8
[97]	2025	3L-FCML, QAM	160	3	4	12.6	2	98.3
[98]	2014	LLC, VPPM	80	3-10	0.047	-	0.47	95.1
[99]	2018	Buck, PSK	22.6	1	0.05	-	0.1	91
[22]	2018	High + Low Frequency Buck, QAM	10.1	0.2	5	12.5	10	91.3
[101]	2020	Re-SC, VPPM	10	1	0.1	-	0.5	85.4
[102]	2021	Buck, coded PWM	4	0.3	1.25	-	0.5	90

5.4.3 Comparison to Other Designs

Table 5.5 compares this work to some recent similar VLC systems designed using switched-mode power converters to power LEDs for wide-angle visible light communication and illumination, listed in order of output power. For works with multiple stages, e.g. low frequency bias circuit + high frequency communication circuit, the switching frequency of the high frequency communication circuit is listed.

The design presented in this chapter stands out from existing works in several ways. First, the output power is an order of magnitude higher, which dramatically extends the communication range and illumination level for large-area Li-Fi applications. At the same time, the bit rate and communication quality at maximum range are also leading for the power level. Fundamentally, these improvements are achieved by the multiphase, multilevel, coupled magnetics architecture that enables a balanced 24× multiplication of the effective switching frequency, enabling high efficiency and high throughput performance simultaneously. The table does not compare area since most designs do not report the converter size; the converter power stage of this chapter, including gate drive and output filter, occupies only 17 cm^2.

5.5 Discussion and Further Improvements

Using a multiphase, multilevel, coupled magnetics architecture, this chapter designs a passively balanced four-phase, seven-level FCML signal-and-power transmitter for VLC that achieves leading power level, throughput, and range. In this section, we discuss improvements that could be made to the design.

1. The design could be improved by using GaN switches and an appropriately scaled-up input voltage. Silicon switches were chosen due to the limitations of low voltage (< 40 V) GaN devices, but the switching speed of GaN devices could improve communication quality and reduce switching losses (considering the frequency dependence of Fig. 5.9). For example, if seven-level multilevel units were still used, the input voltage could be doubled to 160 V and converted with 40 V GaN devices.

2. The temperature rise of the LEDs limited the power level and duration for which the transmitter could be active. The thermal design should be improved by increasing the number of LEDs for the same power level (spreading the power between more devices) and increasing the layout area and the size of the heat sinks.

3. The control resolution of the FPGA, particularly the limited maximum frequency, limited the signal quality due to amplitude quantization and timing granularity. Using a higher frequency controller or analog control would improve signal quality. Moreover, greater resolution and timing budget could allow for more complex modulation schemes, e.g. orthogonal frequency division multiplexing (OFDM), for greater throughput.

5.6 Chapter Summary

This chapter details the theory and design of a multiphase, multilevel, coupled magnetics signal-over-power converter used to drive a long-distance, wide-angle VLC system with high power, efficiency, and throughput. The designed architecture leverages the density of switched capacitor cells in seven-level FCML units, the passive voltage balancing properties of coupled inductors,

and tightly coupled four-phase inductors to achieve a $24\times$ frequency multiplication of the effective switching, sampling, and ripple frequencies. This means the efficiency (95.8%) and output power (1000 W) approach that of a $f_{\text{sw}} = 800$ kHz converter, while the modulation speed and bandwidth approach that of a $f_{\text{eff}} = 19.2$ MHz converter. In an outdoor visible light communication experiment, the transmitter provides 1000 W of LED illumination while also transmitting 32-QAM data 20 meters away at 6.4 Mbps with an RMS EVM of 8.033%, all of which are leading results. The system uses only one 80 V input supply, no external gate driving supply, no power combiner/bias-T/seperate LED bias supply, and drives on-board LEDs.

6

Conclusion

This thesis studies scalable power electronics architectures, showing how the combination of multiplex switching and coupled passives enables robust, balanced frequency multiplication that fundamentally boosts the achievable efficiency and bandwidth of power converters supplying high-performance loads in computing, transportation, communications, and beyond. The analysis frameworks in this work are broadly applicable to many scalable power converter topologies and the theories developed herein are largely application-, component-, load-, and frequency-agnostic.

Chapters 2 and 3 focus on the theory of scalable power architectures. Both chapters develop formal mathematical frameworks for the study of steady-state balancing and internal dynamics of general multiphase and multilevel converters with coupled magnetics, providing a basis for future study. These frameworks are used to achieve two major results: (i) the theoretical and experimental demonstration that coupled magnetics balance multiplex switches, allowing passive balancing of large-scale converters agnostic of size, load, and frequency, and (ii) the analytical, computational, and experimental demonstration of multi-resonant internal dynamics of large-scale converters and their dependence on initial conditions and system structure. These results are translated into practical design guidance for designing balanced, dynamically stable, and high speed converters leveraging multiplex switches and coupled magnetics.

Chapters 4 and 5 apply the theory of the preceding chapters to design state-of-the-art converters that (i) achieve an order-of-magnitude increase in achievable balanced switching frequency multiplication, and (ii) bring the innovations in power architectures to communications engineering and signal-over-power delivery applications. The level of frequency multiplication achieved herein unlocks the potential for above-switching-frequency modulation of the output; this is demonstrated by synthesizing signal frequencies up to 7.68$\times$ higher than the switching frequency. These achievements are complemented by a information theoretical description of the maximum amplitude and frequency of the output signal. Finally, the above-switching-frequency modulation and massive frequency multiplication are leveraged to design a high-efficiency, high speed Li-Fi transmitter. This experiment achieves a state-of-the-art 1000 W power output on

wide-angle LEDs with 95.8% efficiency (including gate drive) while also communicating 32-QAM data at 6.4 Mbps at a distance of 20 meters.

6.1 Future Work

Many future works exist which could contribute to a more complete realization of the vision put forward by this thesis. The idea of power "architecture" is still in its infancy in the realm of power electronics, and still defies formal definition. This thesis has presented scalable power architectures as encompassing a family of converter topologies (e.g. multiphase buck, series capacitor buck, and flying capacitor multilevel converter) that share some common advantages, analysis methods, and understandings. In particular, this thesis focuses on multiplex switching, coupled magnetics, and their interactions, both steady-state (balancing), and dynamic (multi-resonance). Many major factors remain unstudied which would be key to a full definition of a scalable power architecture, for example:

- Reliability is a key concern for all power converters, and it takes on additional dimensions when considering a scalable converter that freely extends in stages, phases, and levels. Each additional switch is another potential failure mode, and the additional probability of failure should be quantified against simpler topologies, and design recommendations made, e.g. required margins, safe operation modes, protection circuits. The dynamic studies in chapter 3 approach this problem in the sense of external perturbations to the system's internal state, but variables such as time, temperature, and yield remain.

- A thorough study of density and volume is wanting. Chapter 4 makes first-order comparisons of semiconductor area with multiplex switching scaling, but a detailed analysis taking into account required device margins, packaging, and interconnects is needed to fully understand the benefits (or drawbacks) of scaling to many phases, levels, and stages.

- The theory could be extended beyond the PWM converters studied herein. The idea of multiplex switching could be expanded to discretely switched power sources in general,

with an output that may not be a PWM controlled dc output; for example, combining discretely toggled RF power sources using multi-inverter discrete backoff (MIDB) [16] bears many similarities to the techniques in this work.

Next, coupled magnetics are the focus of this thesis, but coupled passives in general (e.g. cross connected capacitors [33]) have been shown to have a balancing effect on multiplex switching converters, which could be better understood by extending the theory in chapter 2. Just as coupled magnetics balance multilevel voltages, it could be shown that coupled capacitors (either via switching or as an actual physical device analogous to a coupled inductor) generally balance multiphase currents.

The above-switching-frequency modulation regime unlocked by the practical demonstrations and basic theory in chapter 4 demand further study. Firstly, the theory and practice could be extended to closed-loop control. This would be especially interesting because of the existence of beat-frequency harmonics at and beyond the switching frequency, which could cause unique stability concerns in closed-loop operation. Indeed, now that the modulation frequency can approach and exceed several of the beat frequency harmonics, techniques should be developed to avoid steady-state unbalancing caused at these modulation frequencies.

Finally, implementing the power architectures in this thesis in an integrated circuit has the potential of dramatically improving performance, as the performance of integrated circuits scales much better than discrete switches which need individual packaging, interconnects, and suffer more parasitics. This would also extend the allowable per-switch switching frequency from the 1 MHz domain to 10 MHz and beyond (depending on process), which, combined with frequency multiplication, could approach effective power conversion frequencies above 100 MHz.

A

Appendix: Balancing Scalable Power Architectures using Coupled Magnetics

The contents of this chapter were previously published under D. H. Zhou, J. Čeliković, D. Maksimović, and M. Chen, IEEE Transactions on Power Electronics, 2024.

A.1 Expanded Models for Coupled Inductors

A multiphase coupled inductor integrates multiple windings on a single magnetic core. Fig. A.1 shows an example four-phase coupled inductor. Assuming the core is symmetric and the top and bottom plates have negligible reluctances, the voltages and currents in the inductor can be described using the inductance dual model [26] as

$$N^2 \begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \vdots \\ \frac{di_M}{dt} \end{bmatrix} = \begin{bmatrix} \mathcal{R}_L + \mathcal{R}_C & \mathcal{R}_C & \cdots & \mathcal{R}_C \\ \mathcal{R}_C & \mathcal{R}_L + \mathcal{R}_C & \cdots & \mathcal{R}_C \\ \vdots & \vdots & \ddots & \vdots \\ \mathcal{R}_C & \mathcal{R}_C & \cdots & \mathcal{R}_L + \mathcal{R}_C \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_M \end{bmatrix}. \tag{A.1}$$

Here, i and v are the current through and voltage over each of the M windings. Each winding has N turns and $\mathcal{R}_L$ and $\mathcal{R}_C$ are the side leg and center leg reluctances respectively, as indicated in Fig. A.1. As the center leg reluctance increases or the side leg reluctance decreases, the inductor becomes more coupled. Higher coupling reduces ripple and transient inductance, and also improves voltage balancing capability. Previous works have detailed optimal coupled inductor design in terms of structure [110], loss [54], integration [27], and transient response [5, 26]. Alternatively, we can parameterize the coupled inductor in terms of its leakage inductance L_l and magnetizing inductance L_μ,

$$L_l = \frac{N^2}{\mathcal{R}_L + M\mathcal{R}_C}, \tag{A.2}$$

$$L_\mu = \frac{N^2(M-1)\mathcal{R}_C}{\mathcal{R}_L(\mathcal{R}_L + M\mathcal{R}_C)}. \tag{A.3}$$

L_l determines the transient performance of a coupled inductor converter [5]. As L_μ/L_l increases, the inductors become more tightly coupled.

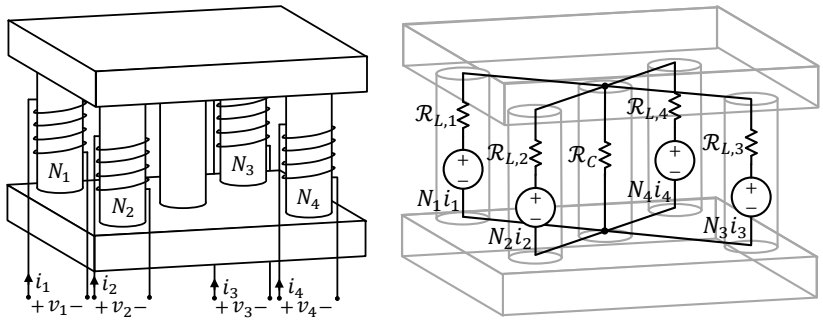


Figure A.1: (a) Drawing of a symmetric four-phase coupled inductor, and (b) reluctance model of a four-phase coupled inductor with center leg reluctance $\mathcal{R}_C$ and side leg reluctances $\mathcal{R}_{L,1} \cdots \mathcal{R}_{L,4}$. The reluctances of the top and bottom plates are neglected in the theoretical analysis. They are not required to be negligible in practical designs.

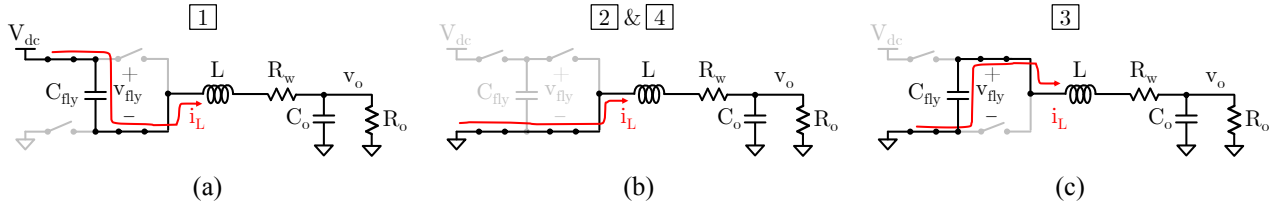


Figure A.2: Equivalent sub-period circuits for the three-level FCML converter.

A.2 Waveform Stitching Technique

As a hybrid switched capacitor system, balancing analysis of FCML converters often involves calculating the inductor current over a switching period with many switching states, each with a different duration and circuit state. Therefore, we compute the solution of each switching state separately and "stitch" them together computationally.

A.2.1 Naturally Balanced FCML Converters

An unbalanced three-level FCML converter has typical switching waveforms shown in Fig. 2.6. There are four switching sub-periods. First, the flying capacitor is connected through V_{dc} to the switch node and it is charged by the inductor current. Second, the switch node is grounded. Third, the flying capacitor is connected through ground to the switch node and it is discharged by the inductor current. Finally, the switch node is grounded again. These switching states are illustrated in Fig. A.2. In this analysis, we assume the duty ratio is smaller than 1/2. Similar analysis can be conducted for other duty ratios with similar results.

In Fig. 2.6, the flying capacitor is assumed to have a positive imbalance, that is, $v_{\text{fly}} > \frac{V_{\text{dc}}}{2}$. Therefore, the switch node has unequal pulse amplitudes. The imbalanced component of the switch node is labelled as $\tilde{v}_{\text{sw}}$. Our goal is to calculate the inductor current induced by this imbalance using the waveform stitching technique and compute the balancing effect and loss.

The imbalanced component of the switch node voltage induces an imbalanced component in the inductor current labelled $\tilde{i}_L$ and is shown for the cases when the winding resistance R_w is zero and nonzero. When the winding resistance is zero, the inductor current ramps linearly and it is obvious that the net charge transfer in the flying capacitor (the shaded areas) is zero. When the winding resistance is nonzero, the inductor current waveform changes exponentially instead of linearly, which is exaggerated in Fig. 2.6 for effect. The flying capacitor is connected in alternating directions and so it sees a negative average current $\tilde{i}_{\text{fly}}$ in both sub-periods #1 and #3.

To quantify the charge transferred into the flying capacitor, we compute the inductor current. We first write the current in each sub-period as a function of the current at the end of the previous sub-period, then solve for the inductor current in each of the sub-period circuits shown in Fig. A.2 as

$$\tilde{i}_L^{\#1}(t) = \tilde{i}_L^{\#4}(d^*T)e^{-\frac{R_w}{L}t} - \frac{\tilde{v}_{\text{fly}}}{R_w}\left(1 - e^{-\frac{R_w}{L}t}\right), \tag{A.4}$$

$$\tilde{i}_L^{\#2}(t) = \tilde{i}_L^{\#1}(dT)e^{-\frac{R_w}{L}t}, \tag{A.5}$$

$$\tilde{i}_L^{\#3}(t) = \tilde{i}_L^{\#2}(d^*T)e^{-\frac{R_w}{L}t} + \frac{\tilde{v}_{\text{fly}}}{R_w}\left(1 - e^{-\frac{R_w}{L}t}\right), \tag{A.6}$$

$$\tilde{i}_L^{\#4}(t) = \tilde{i}_L^{\#3}(dT)e^{-\frac{R_w}{L}t}, \tag{A.7}$$

where $d^* = \frac{1}{2} - d$. For simplicity, each sub-period current is shifted to start at time $t = 0$. Each current is simply the current at the end of the previous sub-period (for example, $\tilde{i}_L^{\#1}(dT)$ is the current at the end of sub-period #1 which is used in the equation for sub-period #2), which decays exponentially, plus a possible forcing function. We need one initial condition to fully define the current. This condition comes from our assumption that the flying capacitance is large so

$\tilde{v}_{\text{fly}}$ does not vary much in a switching period: this means that the average voltage applied to the switch node is zero, and the average inductor current must be zero.

Using the equation of the inductor current with the initial condition applied, we compute the average power loss in the resistor and the charge transferred from the flying capacitor in one period. First, the average power loss in the resistor is

$$\begin{aligned}\left\langle \tilde{P}_{R_w} \right\rangle &= R_w \left\langle \tilde{i_L}^2 \right\rangle \\ &= \frac{R_w}{T} \int_0^T \tilde{i_L}^2 \mathrm{d}t \end{aligned} \tag{A.8}$$

$$\begin{aligned}\left\langle \tilde{P}_{R_w} \right\rangle &\approx \frac{R_w T^2 d^2 \tilde{v}_{\text{fly}}^2 (3-4d)}{12L^2} \\ &= \frac{\gamma}{R_w Q_L^2} \tilde{v}_{\text{fly}}^2. \end{aligned} \tag{A.9}$$

Here, the integral of the square inductor current in (A.8) is calculated symbolically from the inductor current in eq. (A.4) through (A.7). In the final result (A.9), $\gamma = \frac{d^2(3-4d)\pi^2}{3}$ is a scaling factor depending on the duty cycle and $Q_L = \frac{\omega_{\text{sw}} L}{R_w}$ is the quality factor of the inductor at the switching frequency. The power loss is derived by approximating exponential terms with a third-order Taylor series and assuming the quality factor of the inductor is high [64]. The power loss has the general form of a squared voltage divided by the resistance, where the voltage $\frac{\tilde{v}_{\text{fly}}}{Q_L}$ is approximately the voltage over R_w.

The net charge into the flying capacitor during one period is

$$\begin{aligned}\Delta Q &= \int_0^{dT} \tilde{i}_L^{\#1}(t)\,\mathrm{d}t - \int_0^{dT} \tilde{i}_L^{\#3}(t)\,\mathrm{d}t \\ &\approx \frac{\gamma T}{R_w Q_L^2} \tilde{v}_{\text{fly}}, \end{aligned} \tag{A.10}$$

since the capacitor is charged in sub-period #1 and discharged in sub-period #3. The average current into the flying capacitor is therefore

$$\frac{\Delta Q}{T} = \frac{\gamma}{R_w Q_L^2}\tilde{v}_{\text{fly}} = \frac{\left\langle \tilde{P}_{R_w} \right\rangle}{\tilde{v}_{\text{fly}}} = \tilde{i}_{\text{bal}}, \tag{A.11}$$

which is exactly equal to the average power dissipated in the resistor divided by the imbalance voltage, which we define in eq. (2.10) as the balancing current $\tilde{i}_{\text{bal}}$. Therefore, equations (A.8) and (A.11) verify the conclusion in Section 2.3.1 that the small-signal power loss induced by the flying capacitor imbalance relates to the effective flying capacitor balancing current.

A.2.2 Derivation of Timing Factor for Feedback Model of Coupled Inductor Balancing

The same waveform stitching method can be applied to coupled inductor converters. Since coupled inductor balancing does not rely on any losses, the current waveforms are linear, making the analysis much simpler. As explained in Section 2.3, the imbalance voltage of one phase in a two-phase converter will cause a balancing current in the other phase that tends to cancel out disturbances. To mathematically describe this process, we must study the waveforms in detail.

The switching order is important to the balancing behavior. Note that if phase #1 switches "first", that is, connecting to V_{dc} first, then the order of flying capacitors being connected to the switch node is $-\tilde{v}_{\text{fly1}} \rightarrow -\tilde{v}_{\text{fly2}} \rightarrow +\tilde{v}_{\text{fly1}} \rightarrow +\tilde{v}_{\text{fly2}}$, which is not the same should phase #2 be switched "first".

Fig. A.3 shows the balancing waveforms of a two-phase, three-level FCML converter for $d < 0.25$ and phase #1 switching first. We assume that flying capacitor 1 has a positive imbalance voltage. The imbalance voltage of phase #1 induces an imbalance current in phase #2 because of the coupled inductor. During the charging duration of phase #2, which begins at $t = 0.25T$, flying capacitor 2 is charged by

$$Q_{\text{bal}}^{(1,1)\rightarrow(2,1)} = -\frac{(dT)^2 \tilde{v}_{\text{fly1}}}{L_{\text{cross}}}. \tag{A.12}$$

On average, this means that a balancing current of $-\frac{d^2 T \tilde{v}_{\text{fly2}}}{L_{\text{cross}}}$ is applied to phase #2. A positive flying capacitor voltage imbalance in phase #1 will induce a negative balancing current in phase #2

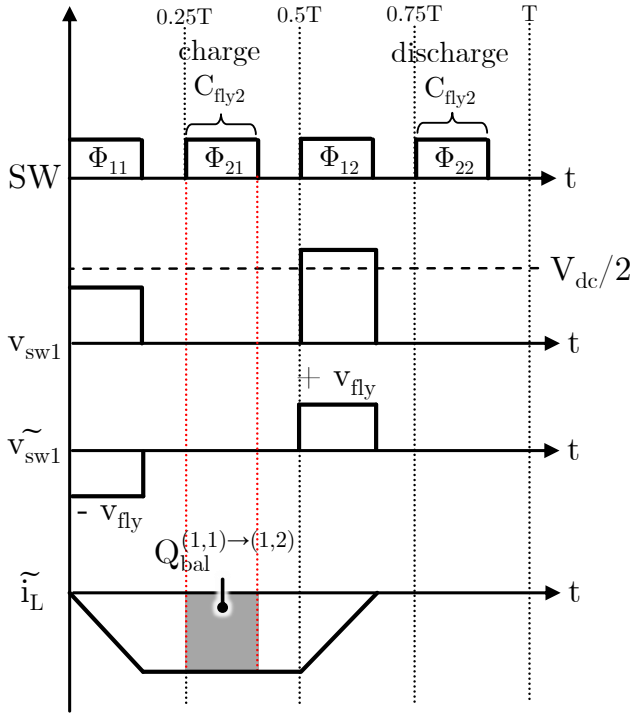


Figure A.3: Switching waveforms of two-phase, three-level FCML converter used to derive the timing factor in the feedback path.

scaled by $\frac{d^2T}{L_{cross}}$, as shown in Fig. 2.9. On the other hand, a similar derivation shows that a positive imbalance in phase #2 induces a positive current in phase #1, so the timing factor is $-d^2T$ in this case. Since one timing factor is negative and one is positive, a full traversal of the loop indicates it is in negative feedback. In summary, the waveform stitching method can easily find the balancing relationships between each phase. In particular, a timing factor must be found to account for the order of switching, duration of sub-periods, and their subsequent effect on the balancing matrix to describe the balancing behavior.

A.3 Derivation of Coupled Inductor Balancing Capabilities for an Arbitrary Number of Phases

If we restrict the duty cycle to $d < \frac{1}{2M}$, the balancing matrix $\mathbf{A}$ takes the form in eq. (2.22). Let $\mathbf{X}$ be

$$\mathbf{X} = \begin{bmatrix} 0 & 1 & 1 & 1 & \cdots & 1 \\ -1 & 0 & 1 & 1 & \cdots & 1 \\ -1 & -1 & 0 & 1 & \cdots & 1 \\ -1 & -1 & -1 & 0 & \cdots & 1 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & -1 & -1 & \cdots & 0 \end{bmatrix}_{M \times M}, \tag{A.13}$$

which is the balancing matrix $\mathbf{A}$ with shared scaling terms factored out. If $\mathbf{X}$ has a nonzero determinant, $\mathbf{A}_{M\text{-phase}}$ is invertible, a solution to eq. (2.18) exists, and the coupled inductor will balance the flying capacitors. $\mathbf{X}$ is skew-symmetric, so if M is odd, $|\mathbf{X}|_{M \text{ odd}} = 0$ [111]. The coupled inductors will not balance the flying capacitors if there are an odd number of phases. If M is even, $|\mathbf{X}| = 1$. Therefore, the balancing matrix is always invertible for an even number of phases M and the coupled inductors can balance the flying capacitors.

To estimate how the balancing strength scales with the number of phases, we compute the inverse of $\mathbf{A}$ if M is even. The inverse of $\mathbf{X}$ is

$$\mathbf{X}^{-1} = \begin{bmatrix} 0 & -1 & 1 & -1 & \cdots & -1 \\ 1 & 0 & -1 & 1 & \cdots & 1 \\ -1 & 1 & 0 & -1 & \cdots & -1 \\ 1 & -1 & 1 & 0 & \cdots & 1 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & -1 & 1 & -1 & \cdots & 0 \end{bmatrix}_{M \times M}, \tag{A.14}$$

and for a given imbalance vector $\mathbf{Q}_{\text{dist}}$, the steady-state voltage imbalances are

$$\begin{aligned} \tilde{\mathbf{v}}_{\text{fly}} &= -\mathbf{A}^{-1}\mathbf{Q}_{\text{dist}} \\ &= \frac{L_{\text{cross}}}{(dT)^2}\mathbf{X}^{-1}\mathbf{Q}_{\text{dist}}. \end{aligned} \tag{A.15}$$

For a time shift disturbance where each phase has a time shift of Δt_m for $m = 1, \ldots, M$, the disturbance vector is

$$\mathbf{Q}_{\text{dist}} = dT \times \frac{dV_{\text{dc}}}{L_l} \begin{bmatrix} \Delta t_1 \\ \Delta t_2 \\ \Delta t_3 \\ \vdots \\ \Delta t_M \end{bmatrix}, \tag{A.16}$$

following from the derivation in the four phase case in Section 2.4. Assuming each time shift has a maximum magnitude of Δt and is either positive or negative (lag or lead respectively), we can compute the best- and worst- case imbalance depending on the signs of the time shifts. Without loss of generality, we consider the first flying capacitor. If all the time shifts are in the same direction, then the flying capacitor voltage imbalance is

$$\begin{aligned} \tilde{\mathbf{v}}_{\text{fly}} &= \frac{L_{\text{cross}}}{(dT)^2}\mathbf{X}^{-1} \times dT\frac{dV_{\text{dc}}}{L_l} \begin{bmatrix} \Delta t \\ \Delta t \\ \Delta t \\ \vdots \\ \Delta t \end{bmatrix} \\ \rightarrow \tilde{v}_{\text{fly}}^{(1,1)}\Big|_{\text{best-case}} &= \frac{V_{\text{dc}}\Delta t L_{\text{cross}}}{TL_l}. \end{aligned} \tag{A.17}$$

In the worst case, the direction of the time shifts alternates. In this case, the worst-case imbalance of capacitor #1 is

$$\begin{aligned} \tilde{\mathbf{v}}_{\text{fly}} &= \frac{L_{\text{cross}}}{(dT)^2}\mathbf{X}^{-1} \times dT\frac{dV_{\text{dc}}}{L_l} \begin{bmatrix} +\Delta t \\ -\Delta t \\ +\Delta t \\ \vdots \\ -\Delta t \end{bmatrix} \\ \rightarrow \tilde{v}_{\text{fly}}^{(1,1)}\Big|_{\text{worst-case}} &= \frac{(M-1)V_{\text{dc}}\Delta t L_{\text{cross}}}{TL_l}. \end{aligned} \tag{A.18}$$

A.4 Derivation of Coupled Inductor Balancing Capabilities for an Arbitrary Number of Levels

We compute the balancing matrix of a two-phase, $(K+2)$-level converter, which has switching waveforms shown in Fig. 2.13. First, consider the charge transfers that capacitor #1 of phase #1 induces:

$$Q_{\text{bal}}^{(1,1)\to(1,2)} = (dT)^2 \frac{1}{2L_{\text{same}}} \tilde{v}_{\text{fly}}^{(1,1)} \tag{A.19}$$

in capacitor #2 of phase #1 and

$$Q_{\text{bal}}^{(1,1)\to(2,1)} = (dT)^2 \frac{1}{L_{\text{cross}}} \tilde{v}_{\text{fly}}^{(1,1)} \tag{A.20}$$

in capacitor #1 of phase #2. A similar pattern exists for the charge transfers of the other flying capacitors, with scaling by the cross inductance for charge induced in the other phase and scaling by the self inductance for charge induced in the other capacitors of the same phase. If we extend this to $(K+2)$-levels per phase and $d < \frac{1}{2(K+1)}$, the balancing matrix $\mathbf{A}$ takes the form in eq. (2.29) with α and β as the element values. $\mathbf{A}_{\text{(K+2)-levels}}$ is size $2K \times 2K$ since there are two phases with K flying capacitors each. The balancing matrix is skew-symmetric, pentadiagonal, of even size, and Toeplitz, and if $\beta \neq 0$, it has the determinant

$$|\mathbf{A}_{\text{(K+2)-levels}}| = \left[\beta^K U_K(x)\right]^2, \tag{A.21}$$

where U_K is the Chebyshev polynomial of the second kind of degree K and the argument being the coupling ratio

$$x = \frac{\alpha}{2\beta} = \frac{L_{\text{same}}}{L_{\text{cross}}} = \frac{k}{M-1+k} \in (0,1]. \tag{A.22}$$

Eq. (A.21) indicates that the balancing matrix is singular only at the roots of U_K, which are

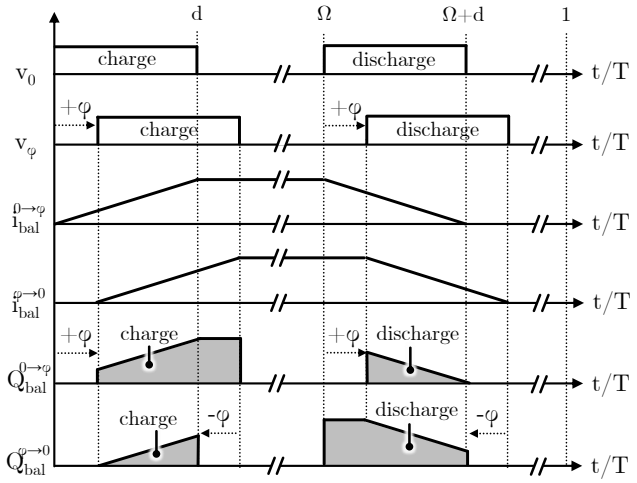


Figure A.4: General charge transfer behavior between two arbitrary phase-shifted flying capacitors in a coupled inductor FCML system.

$$x_j = \cos\left(\frac{j}{K+1}\pi\right) \tag{A.23}$$

for $j = 1, \ldots, K$. The largest root of U_K is at $x_1 = \cos\left(\frac{1}{K+1}\pi\right)$. If the converter coupling ratio x is equal to any of the roots in eq. (A.23), the converter will not balance. With fully coupled inductors, the coupling ratio $x = \frac{L_{\text{same}}}{L_{\text{cross}}} \to 1$, which is greater than all of the roots in (A.23), meaning fully coupled inductors can balance any finite number of levels. For partially coupled inductors with $\frac{L_{\text{same}}}{L_{\text{cross}}} < 1$, a sufficient condition on the coupling ratio to avoid coinciding with all roots is

$$x = \frac{L_{\text{same}}}{L_{\text{cross}}} > x_1 = \cos\left(\frac{1}{K+1}\pi\right). \tag{A.24}$$

As the number of levels increases, the largest root x_1 and required coupling ratio increase.

A.5 Singularities of the Balancing Matrix

Previously, we only considered specific operating conditions and level/phase combinations to explain coupled inductor balancing. However, the balancing matrix of an M-phase and $(K+2)$-level FCML converter can have arbitrarily large order and any duty cycle and coupling ratio. In this section, we generalize balancing behavior for any operating conditions from the structure of the balancing matrix.

A.5.1 Toeplitz and Skew-Symmetric Properties of the Balancing Matrix

Assuming that the phase shifts between all switches are uniform, the balancing matrix is always Toeplitz and skew-symmetric. To prove this, we consider without loss of generality a flying capacitor called v_0 being connected to the switch node (labelled in Fig. A.4), assuming its phase to be zero. This flying capacitor could be from any switching level of a $(K+2)$-level converter. Every flying capacitor is connected with equal duration in the both a positive and negative orientations in order to maintain charge balancing. In Fig. A.4, the phase shift between the flying capacitor being connected again is Ω.

Now we analyze the charge transfer that the flying capacitor induces in another flying capacitor that has its switching actions phase shifted by ϕ which we call v_ϕ, and the charge that v_ϕ induces in v_0. Fig. A.4 shows the small-signal imbalance currents and charges induced by each of the flying capacitors in the other. By inspection, we can see that the two flying capacitors are charged and discharged with the same magnitude and opposite signs. Therefore, we can conclude that if a first flying capacitor v_0 induces a charge Q in a flying capacitor v_ϕ, then flying capacitor v_ϕ induces a charge of $-Q$ in v_0. This is equivalent to saying the balancing matrix must be skew symmetric, since all symmetric entries about the diagonal will have equal magnitude and inverted sign. This proof is uniform across the full operation range and does not depend on the phase shift between the charging and discharging pulses (Ω), the phase shift between the two capacitors (ϕ), or the duty cycle regime.

We now prove that the balancing matrix is Toeplitz. If a flying capacitor, say our base capacitor v_0, causes a charge transfer Q in another that is phase shifted by ϕ, then all the flying capacitors will cause the same charge transfer Q in the flying capacitor phase shifted by ϕ from them. This is a consequence of the symmetry of the converter and the fact that the switching actions are all uniform with equal phase shift. The entries on the same balancing matrix diagonals correspond to equal phase shifts between the flying capacitors, so we can conclude that the balancing matrix must be Toeplitz.

A.5.2 Polynomial Determinant of the Balancing Matrix

Generally, each element of the balancing matrix is a polynomial of d scaled by either the L_{cross} or L_{same} inductance. We consider d as a variable and the inductances as fixed since a converter generally has a fixed coupled inductor but can operate across the entire duty cycle regime. Given the varying elements and arbitrary size of $MK \times MK$, it is difficult to explicitly prove the invertibility, and therefore the balancing capability, of the balancing matrix in all cases. However, we can use the skew-symmetric property of the balancing matrix to place bounds on the balancing capability.

First, the determinant of a skew-symmetric matrix of even order can be expressed as a square of a polynomial of its elements [111]. Since the elements are themselves polynomials of d, we know that the determinant of the balancing matrix is a square of a polynomial in d

$$|\mathbf{A}| = \left(p\left(d\right)\right)^2, \tag{A.25}$$

where p is a polynomial. The degree of the elements of $\mathbf{A}$ can be as large as 2 in d, since the charge transfer elements are calculated as an "area" where the sides are both dependent on the duty cycle. Therefore, as MK is the size of $\mathbf{A}$, the degree of the polynomial $|\mathbf{A}|$ can be as large as $2MK$ in d, and the degree of $p(d)$ can be as large as MK in d.

At the roots of $p(d)$, the balancing matrix is singular and balancing fails. Since $p(d)$ is a univariate polynomial of d with degree MK, there are at most MK roots which are generally discrete complex values of d.

A.5.3 Limiting Singularities of the Balancing Matrix

The dependence of the balancing matrix on duty cycle changes abruptly at the "nominal" conversion ratios defined in [46] that are multiples of $\frac{1}{M(K+1)}$. There are generally $M(K+1)$ unique operating regions of the duty cycle bounded by these nominal conversion ratios. The behavior of different regions generally changes when crossing these boundaries because the number of overlapping on-switches changes. The reason there are $M(K+1)$ regions is because there are a total

of $M(K+1)$ total switching actions during a switching period, so one phase can overlap between 0 and $(M(K+1)-1)$ other actions, for a total of $M(K+1)$ possibilities.

To explain the different balancing behavior in each duty cycle region, we define i as an index representing the duty cycle operating region of an M-phase, $(K+2)$-level converter, where the duty cycle in operating region i is in the range $\frac{i-1}{M(K+1)} < d \leq \frac{i}{M(K+1)}$ (bounded by the two nearest nominal conversion ratios). Since there are $M(K+1)$ unique regions, the index can take the values $i = 1, 2, \ldots M(K+1)$. Formally, the definition of i is

$$i = \text{ceil}(M(K+1)d). \tag{A.26}$$

We now rewrite the charge balancing equation (2.18) with explicit reference to the operating region i as

$$\mathbf{Q}_{\text{bal}} + \mathbf{Q}_{\text{dist}} = \mathbf{A}_i(d)\tilde{\mathbf{v}}_{\text{fly}} + \mathbf{Q}_{\text{dist}} = \mathbf{Q}_{\text{cap}}. \tag{A.27}$$

As with before, we assume there is a generic disturbance charge $\mathbf{Q}_{\text{dist}}$ injected on the flying capacitors and a balancing charge $\mathbf{Q}_{\text{bal}}$ that counters it. The balancing matrix is now written as $\mathbf{A}_i(d)$, where i is the operating region and the dependence on the duty cycle d is highlighted. Finally, the sum of the balancing and disturbance charges is not automatically assumed to be zero, but rather an explicit excess capacitor charge $\mathbf{Q}_{\text{cap}}$. This highlights the fact that if $\mathbf{A}_i(d)$ is singular for a given duty cycle, then it will not be possible to cancel out an arbitrary disturbance.

We can now formally define the duty cycles, if any exist, when balancing fails. Coupled inductor balancing fails for the set of duty cycles

$$\mathcal{D} = \{d \in (0,1) \,||\mathbf{A}_i(d)| = 0\}. \tag{A.28}$$

We only consider purely real values of d strictly between 0 and 1 since these are the only non-trivial switching regions. $\mathcal{D}$ specifies all duty cycles in this range which cause the determinant of the corresponding balancing matrix to be zero, which indicates a failure of balancing capability.

There are at most MK roots of $|\mathbf{A}_i(d)| = 0$ for each i. If a root falls within the range $\frac{i-1}{M(K+1)} < d \leq \frac{i}{M(K+1)}$, then that root is in $\mathcal{D}$. If the root falls outside this region or is complex, it is not a practically achievable duty cycle and is not a singularity. Since there are at most MK roots per region i that could be in $\mathcal{D}$, and $M(K+1)$ total regions, the maximum number of singularities is

$$n(\mathcal{D}) \leq M^2K(K+1), \tag{A.29}$$

where $n(\mathcal{D})$ is the number of elements in $\mathcal{D}$. Meanwhile, the maximum number of singularities within a particular duty cycle region defined by i is $n_i \leq MK$.

These results imply that for a finite number of levels and phases, there is a finite maximum number of duty cycle singularities that can exist, meaning that balancing will generally be possible across the entire duty cycle regime except at specific singular points. We can also conclude that as the number of phases and levels increases, the maximum number of singularities within each duty cycle region i increases while the size of each duty cycle region decreases. Since there are more possible singularities in a smaller space as M and K increase, it is possible that balancing fails for all duty cycles as the number of phases $M \to +\infty$ and/or levels $(K+2) \to +\infty$.

A.5.4 Computation of Singularities for Four-Phase Converter

We compute the singularities of a four-phase, three-level FCML converter with $\frac{1}{4} < d \leq \frac{3}{8}$. The balancing matrix in the $i = 3$ operating region may be computed as

$$\mathbf{A}_{i=3}(d) = \frac{T^2}{L_{\text{cross}}} \begin{bmatrix} 0 & \alpha & \beta & \alpha \\ -\alpha & 0 & \alpha & \beta \\ -\beta & -\alpha & 0 & \alpha \\ -\alpha & -\beta & -\alpha & 0 \end{bmatrix}, \tag{A.30}$$

where

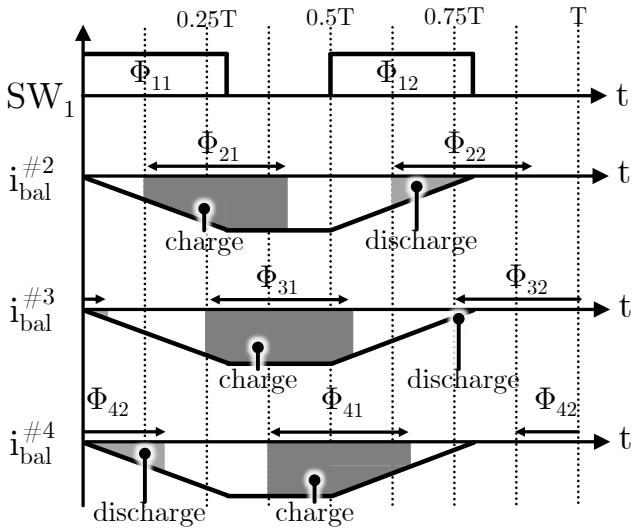


Figure A.5: Balancing currents induced by phase #1 in a four-phase, three-level FCML converter with coupled inductors when the duty cycle is in the range $\frac{1}{4} < d < \frac{3}{8}$.

$$\alpha = \frac{d}{8} + \frac{1}{8}\left(d - \frac{1}{8}\right), \tag{A.31}$$

$$\beta = d^2 - 2\left(d - \frac{1}{4}\right)^2. \tag{A.32}$$

After computing the determinant and numerically finding the roots of the resulting polynomial of d, we find the set of singular duty cycles for the four-level converter is

$$\mathcal{D} = \{0.2836, 0.3629\}. \tag{A.33}$$

Coupled inductor cannot help with balancing the flying capacitor voltages at these two singular duty cycles.

B

Appendix: Demystifying the Multi-Resonant Dynamics of Large-Scale Power Architectures

The contents of this chapter were previously published under D. H. Zhou and M. Chen, IEEE Transactions on Power Electronics, 2025.

B.1 Derivation of Power Dissipation Balancing Model

We restrict our analysis to three-level converters. There are generally $4M$ sub-periods, each with a different switching state. During each state, the inductor current is linearly ramped up or down by the connected flying capacitors. Because the starting current in each sub-period depends on the changes that occur in the preceding sub-periods, we define the current in each sub-period sequentially as

$$\tilde{i}_{L,j}(t) = \begin{cases} \frac{\mathbf{S}_1 \tilde{\mathbf{v}}_{\text{fly}}}{L_l} t - \tilde{i}_{\text{offset}} & j = 1 \\ \tilde{i}_{L,j-1}\big|_{t=d^* T} + \frac{\mathbf{S_j} \tilde{\mathbf{v}}_{\text{fly}}}{L_l} t & j \text{ odd}, j \neq 1 \\ \tilde{i}_{L,j-1}\big|_{t=d_{\text{rem}} T} + \frac{\mathbf{S_j} \tilde{\mathbf{v}}_{\text{fly}}}{L_l} t & j \text{ even}. \end{cases} \tag{B.1}$$

The switch state vector $\mathbf{S_j}$ is defined in section B.2. The current in sub-period #1 ramps due to the connected flying capacitors, defined by $\mathbf{S}_1 \tilde{\mathbf{v}}_{\text{fly}}$, minus a starting offset $\tilde{i}_{\text{offset}}$. The current in every subsequent sub-period is the current at the end of the previous sub-period plus a ramp. All the sub-period currents are assumed to start at $t = 0$ for simplicity. The initial condition for eq. (B.1) is found by setting the average inductor current to zero

$$\sum_{j=1}^{j=4M} \int_0^{t_j} \tilde{i}_{L,j}(t) \mathrm{d}t = 0 \tag{B.2}$$

and solving for the necessary offset current $\tilde{i}_{\text{offset}}$ which we substitute into eq. (B.1). The average power loss incurred in an unbalanced converter compared to a balanced converter is

$$\begin{aligned} R_w \left\langle i_L(t)^2 \right\rangle &= \frac{R_w}{T} \left[\sum_{j=1}^{j=4M} \int_0^{t_j} \tilde{i}_j(t)^2 \mathrm{d}t \right] \\ &= \frac{R_w T^2}{L_l^2} \times X\left(d, \tilde{\mathbf{v}}_{\text{fly}}(t)\right). \end{aligned} \tag{B.3}$$

The loss is a function of the duty cycle and flying capacitor voltages, which we represent with the function X. For a single-phase, three-level converter with $d < 0.5$ (mirrored for $d \geq 0.5$), the function is

$$X_{M=1} = \frac{d^2(3-4d)\tilde{v}_{\text{fly}}(t)^2}{12}. \tag{B.4}$$

For a two-phase, three-level converter with $d < 0.5$, it is

$$\begin{aligned} X_{M=2} &= \frac{d^2(3-4d)\left[(\tilde{v}_{\text{fly,1(t)}})^2 + (\tilde{v}_{\text{fly,2(t)}})^2\right]}{24} \\ &= \frac{d^2(3-4d)\|\tilde{\mathbf{v}}_{\text{fly}}(t)\|^2}{24}. \end{aligned} \tag{B.5}$$

B.2 Derivation of State-Space Model

To derive a generalized dynamic model for the flying capacitor voltages, we first define the relevant variables. If there are M phases and K flying capacitors per phase, there are $M \times K$ flying capacitor voltages

$$\tilde{\mathbf{v}}_{\text{fly}} = \begin{bmatrix} \tilde{v}_{\text{fly}}^{(1,1)} & \tilde{v}_{\text{fly}}^{(1,2)} & \cdots & \tilde{v}_{\text{fly}}^{(1,K)} & \tilde{v}_{\text{fly}}^{(2,1)} & \cdots & \tilde{v}_{\text{fly}}^{(M,K)} \end{bmatrix}^{\text{T}}. \tag{B.6}$$

Ideally, the state vector $\tilde{\mathbf{v}}_{\text{fly}} = 0$ if there are no imbalances. The full state vector, defined below as $\tilde{\mathbf{x}}$, also includes one state for the inductor current for each phase:

$$\tilde{\mathbf{x}} = \begin{bmatrix} \tilde{\mathbf{v}}_{\text{fly}} \\ \tilde{i}_L \end{bmatrix}, \tag{B.7}$$

The flying capacitor voltages are connected differently during each switching state of the converter. To represent these changes, we define a switch state vector $\mathbf{j}$ for each switching state as

$$\mathbf{j} = \begin{bmatrix} \Phi_j^{(1,1)} & \cdots & \Phi_j^{(1,K+1)} & \Phi_j^{(2,1)} & \cdots & \Phi_j^{(M,K+1)} \end{bmatrix}, \tag{B.8}$$

where $\Phi_j^{(m,k'))}$ is the state of switch (m,k') for switching state j and is either 1 (ON) or 0 (OFF).

$j = 1, 2, \ldots, 2M(K+1)$ denotes the switching state. From the switch state vector, we can determine how (or if) each flying capacitor is connected to the output during a given switching state. We let the flying capacitor state vector be

$$\mathbf{S_j} = \begin{bmatrix} S_j^{(1,1)} & S_j^{(1,2)} & \cdots & S_j^{(1,K)} & S_j^{(2,1)} & \cdots & S_j^{(M,K)} \end{bmatrix}, \tag{B.9}$$

where the flying capacitor with index (m, k) has connection

$$S_j^{(m,k)} = \Phi_j^{(m,k+1)} - \Phi_j^{(m,k)} \tag{B.10}$$

during sub-period j. If both adjacent switches have the same state, the capacitor is disconnected with $S_j^{(m,k)} = 0$. If not, $S_j^{(m,k)} = \pm 1$, representing the orientation of the flying capacitor. The sum of all the flying capacitor voltages connected to the output is

$$\tilde{v}_{\text{sum}} = \sum_{m=1}^{M} \sum_{k=1}^{K} S_j^{(m,k)} \tilde{v}_{\text{fly}}^{(m,k)} = \mathbf{S_j} \begin{bmatrix} \tilde{v}_{\text{fly}}^{(1,1)} \\ \tilde{v}_{\text{fly}}^{(1,2)} \\ \vdots \\ \tilde{v}_{\text{fly}}^{(M,K)} \end{bmatrix} \tag{B.11}$$

We now write the differential equations of the circuit, starting with the flying capacitors,

$$\frac{\mathrm{d}\tilde{v}_{\text{fly}}^{(m,k)}}{\mathrm{d}t} = -S_j^{(m,k)} \frac{1}{C_{\text{fly}}} \frac{\tilde{i}_L}{M}, \tag{B.12}$$

where the connection state $S_j^{(m,k)}$ determines if the capacitor charges or discharges. After the reduction in Fig. 3.6, we write the equation for the output network as

$$\tilde{v}_{\text{sum}} - L_l \frac{\mathrm{d}\tilde{i}_L}{\mathrm{d}t} - R_w \tilde{i}_L = 0. \tag{B.13}$$

Assuming at least one flying capacitor is connected to the output, we take the derivative of eq. (B.13) and substitute eqs. (B.11) and (B.12) into it, obtaining

$$\sum_{m=1}^{M}\sum_{k=1}^{K} S_j^{(m,k)} \frac{\mathrm{d}\tilde{v}_{\text{fly}}^{(m,k)}}{\mathrm{d}t} - L_l \frac{\mathrm{d}^2\tilde{i}_L}{\mathrm{d}t^2} - R_w \frac{\mathrm{d}\tilde{i}_L}{\mathrm{d}t} = 0$$

$$\frac{\mathrm{d}^2\tilde{i}_L}{\mathrm{d}t^2} + \frac{R_w}{L_l}\frac{\mathrm{d}\tilde{i}_L}{\mathrm{d}t} + \frac{1}{L_l C_{\text{fly}} M}\tilde{i}_L \sum_{m=1}^{M}\sum_{k=1}^{K}\left|S_j^{(m,k)}\right| = 0$$

$$\frac{\mathrm{d}^2\tilde{i}_L}{\mathrm{d}t^2} + a\frac{\mathrm{d}\tilde{i}_L}{\mathrm{d}t} + b\tilde{i}_L = 0, \tag{B.14}$$

where

$$a = \frac{R_w}{L_l}; b = \frac{1}{ML_l\left(C_{\text{fly}}/n_j\right)}. \tag{B.15}$$

Here, the term $n_j = \sum_{m=1}^{M}\sum_{k=1}^{K}\left|S_j^{(m,k)}\right|$ is the number of flying capacitors connected to the output during sub-period j, regardless of orientation. Equation (B.14) has the solution

$$\tilde{i}_L(t) = e^{-\frac{a}{2}t}\left[k_1\cos(\omega_d t) + k_2\sin(\omega_d t)\right], \tag{B.16}$$

where $\omega_d = \frac{1}{2}\sqrt{4b - a^2}$ and k_1 and k_2 are constants. k_1 is found by setting $t = 0$ for the beginning of the sub-period, $k_1 = \tilde{i}_L(0)$. Next, taking the derivative of eq. (B.16) and setting it equal to the initial change in inductor current $\frac{\mathrm{d}\tilde{i}_L(0)}{\mathrm{d}t}$, we solve for k_2 as

$$\frac{\mathrm{d}\tilde{i}_L(0)}{\mathrm{d}t} = -\frac{a}{2}k_1 + k_2\omega_d = \frac{1}{L_l}\left[\tilde{v}_{\text{sum}}(0) - R_w\tilde{i}_L(0)\right]$$

$$k_2 = \frac{1}{L_l\omega_d}\tilde{v}_{\text{sum}}(0) - \frac{a}{2\omega_d}\tilde{i}_L(0). \tag{B.17}$$

Substituting the constants into into eq. (B.16), we find the solution for the inductor current in terms of the initial states

$$\tilde{i}_L(t) = \alpha(t)\tilde{v}_{\text{sum}}(t) + \beta(t)\tilde{i}_L(0), \tag{B.18}$$

where

$$\begin{aligned}\alpha(t) &= \frac{1}{\omega_d L_l} e^{-\frac{a}{2}t} \sin(\omega_d t), \\ \beta(t) &= e^{-\frac{a}{2}t} \left[\cos(\omega_d t) - \frac{a}{2\omega_d} \sin(\omega_d t) \right].\end{aligned} \tag{B.19}$$

If no flying capacitors are connected to the output, the inductor current simply decays exponentially through the resistance as $\tilde{i}_L(t) = \tilde{i}_L(0) e^{\frac{R_w}{L_l} t}$. We solve for the flying capacitor voltages by integrating the solution for the inductor current:

$$\begin{aligned}\tilde{v}_{\text{fly}}^{(m,k)}(t) &= -\frac{S_j^{(m,k)}}{M C_{\text{fly}}} \int \tilde{i}_L \, \mathrm{d}t \\ &= A(t)\tilde{v}_{\text{sum}}(0) + B(t)\tilde{i}_L(0) + k_3,\end{aligned} \tag{B.20}$$

where

$$\begin{aligned}A(t) + d_1 &= -\frac{S_j^{(m,k)}}{M C_{\text{fly}}} \int \alpha(t) \, \mathrm{d}t \\ &= \frac{S_j^{(m,k)}}{n_j} e^{-\frac{a}{2}t} \left[\cos(\omega_d t) + \frac{a}{2\omega_d} \sin(\omega_d t) \right] + d_1,\end{aligned} \tag{B.21}$$

$$\begin{aligned}B(t) + d_2 &= -\frac{S_j^{(m,k)}}{M C_{\text{fly}}} \int \beta(t) \, \mathrm{d}t \\ &= -\frac{S_j^{(m,k)}}{M C_{\text{fly}} \omega_d} e^{-\frac{a}{2}t} \sin(\omega_d t) + d_2.\end{aligned} \tag{B.22}$$

The constant k_3 absorbs the constants d_1 and d_2 in eq. (B.20) and is solved for at $t = 0$ as

$$k_3 = \tilde{v}_{\text{fly}}^{(m,k)}(0) + \frac{1}{n_j} \tilde{v}_{\text{sum}}(0). \tag{B.23}$$

Substituting eq. (B.23) into eq. (B.20), we find the solution for the flying capacitor voltage is

$$\tilde{v}_{\text{fly}}^{(m,k)}(t) = \tilde{v}_{\text{fly}}^{(m,k)}(0) + \left[A(t) + \frac{1}{n_j} \right] \tilde{v}_{\text{sum}}(0) + B(t)\tilde{i}_L(0). \tag{B.24}$$

Equation (B.18) and eq. (B.24) are used to update the inductor current and flying capacitor voltages from the initial states during a sub-period. In these equations, the time t refers to the time elapsed from when the sub-period begins at $t = 0$. Therefore, if we substitute $t = \Delta t_j$, where Δt_j is the duration of the sub-period, equations (B.18) and eq. (B.24) give the states at the end of the sub-period. Since an update equation exists for all the state variables, we can write a state transition equation

$$\mathbf{x}(\Delta t) = \mathbf{T_j}(\Delta t_j)\mathbf{x}(0), \tag{B.25}$$

where $\mathbf{T_j}(\mathbf{t})$ is the transition matrix for sub-period j. Note that the sub-period transition matrix is only dependent on the switch states and the other coefficients do not need to be recomputed. By computing the state transition matrix for every sub-period and multiplying them together in the order they occur, we can update the state variables from the beginning to the end of a period as

$$\mathbf{x}(T) = \left(\prod_{j=1}^{2M(K+1)} \mathbf{T_j}(\Delta t_j) \right) \mathbf{x}(0) = \mathbf{T}_{\text{full}}\mathbf{x}(0). \tag{B.26}$$

where Δt_j is the sub-period duration

$$\Delta t_j = \begin{cases} d^* T & j \text{ odd} \\ \left(\frac{1}{M(K+1)} - d^* \right) T & j \text{ even} \end{cases}. \tag{B.27}$$

To perform continuous-time analysis on the dynamic model, we use an approximation of the derivative assuming the balancing dynamics are much slower than the switching frequency. In this work, we use the second order central approximation of the derivative,

$$\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}t} \approx \frac{-\mathbf{T}_{\text{full}}{}^2 + 8\mathbf{T}_{\text{full}} - 8\mathbf{T}_{\text{full}}{}^{-1} + (\mathbf{T}_{\text{full}}{}^{-1})^2}{12T}\mathbf{x}(t) = \mathbf{A}\mathbf{x}(t). \tag{B.28}$$

The continuous-time state matrix $\mathbf{A}$ determines the flying capacitor voltage balancing dynamics of the converter.

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