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Implementing Vertical Power Delivery for AI Processors

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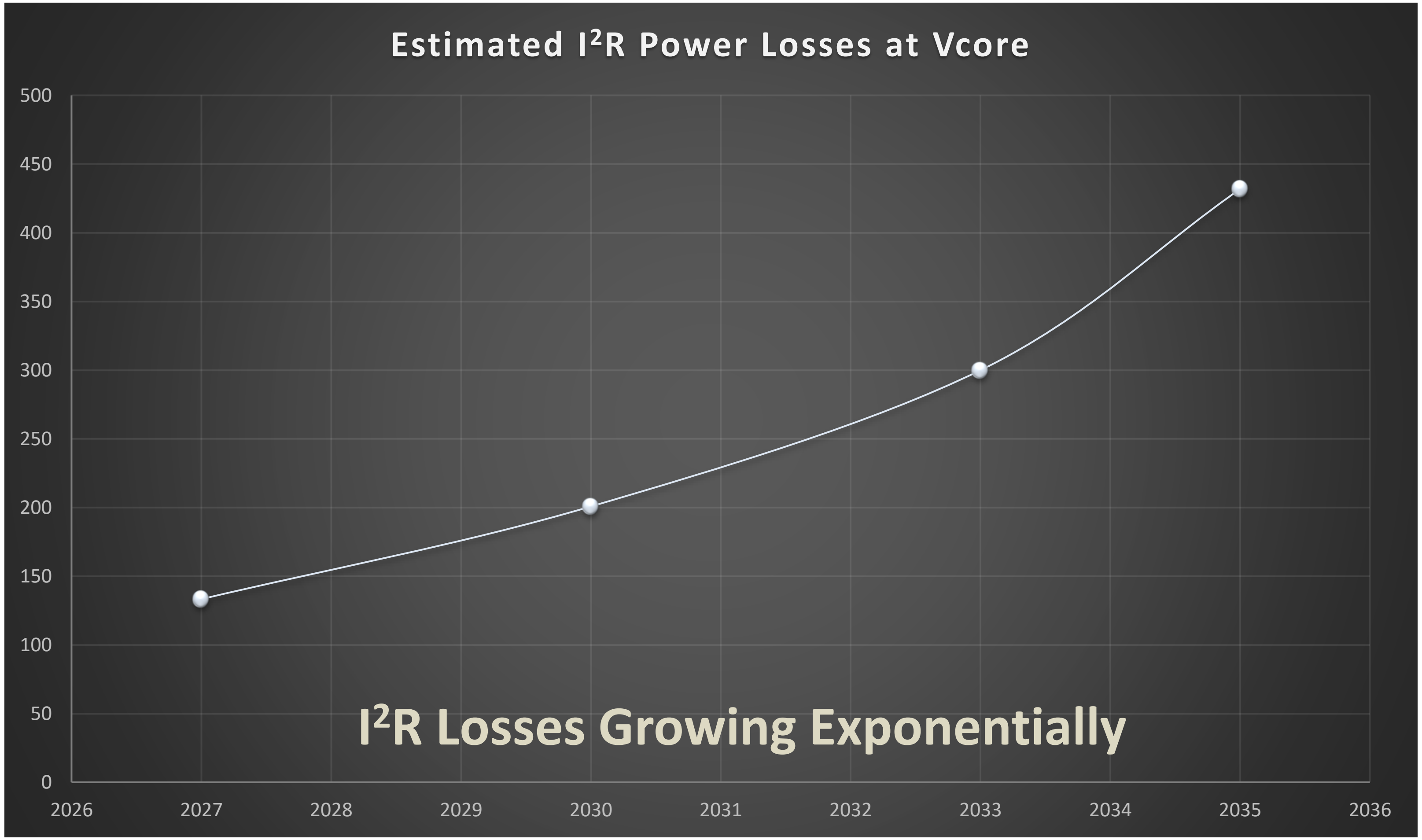
Unleash Innovation

1: TSMC Incorporated
2: Princeton University

Outline of this Talk

- Need for Vertical Power Delivery
- Benefits of Integrated Voltage Regulators
- Ingredients for successful Implementation
- Wrap-Up with Q&A

Why: Projected Current Density



Losses based on extrapolated data from various sources and is not based on any system

Benefits of Vertically In-Package Regulators

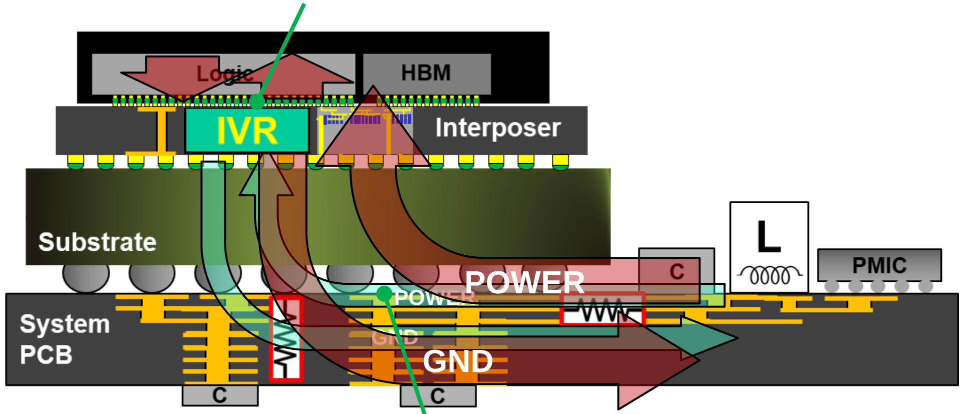
$$P_{loss} = I^2 R$$

- Lowers I^2R loss
- Reduce EM constrain in power path

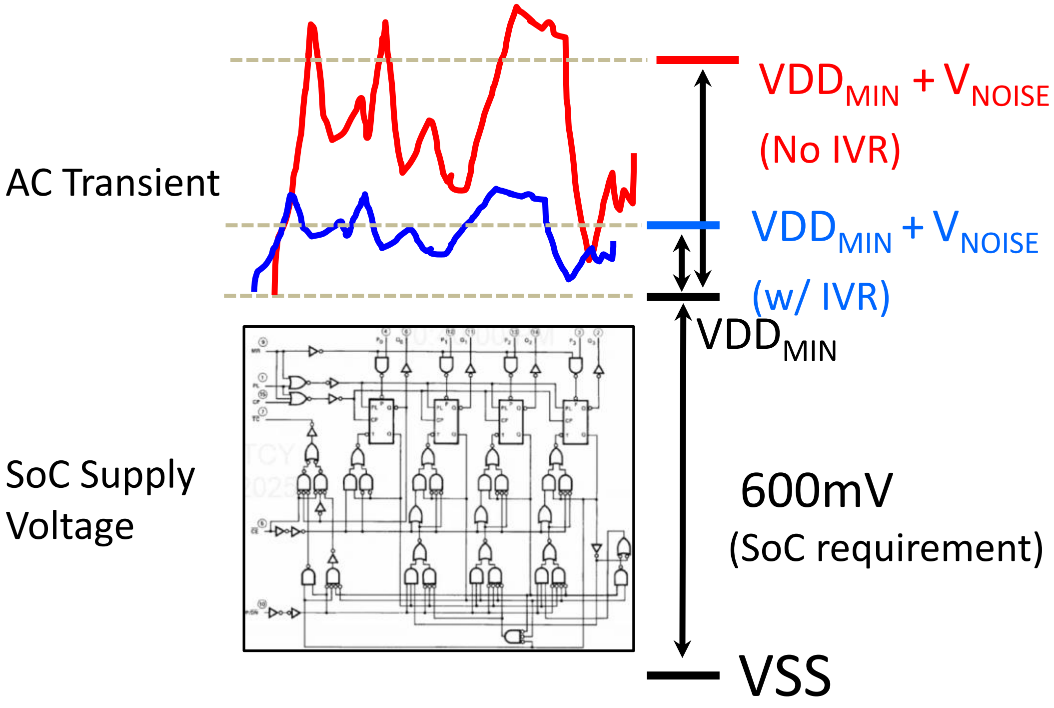
$$P_{SoC} = \frac{1}{2} C V^2 F$$

- Reduces Inductance Loop
- Lower transient noise ➔ Lower VDD_{MIN}

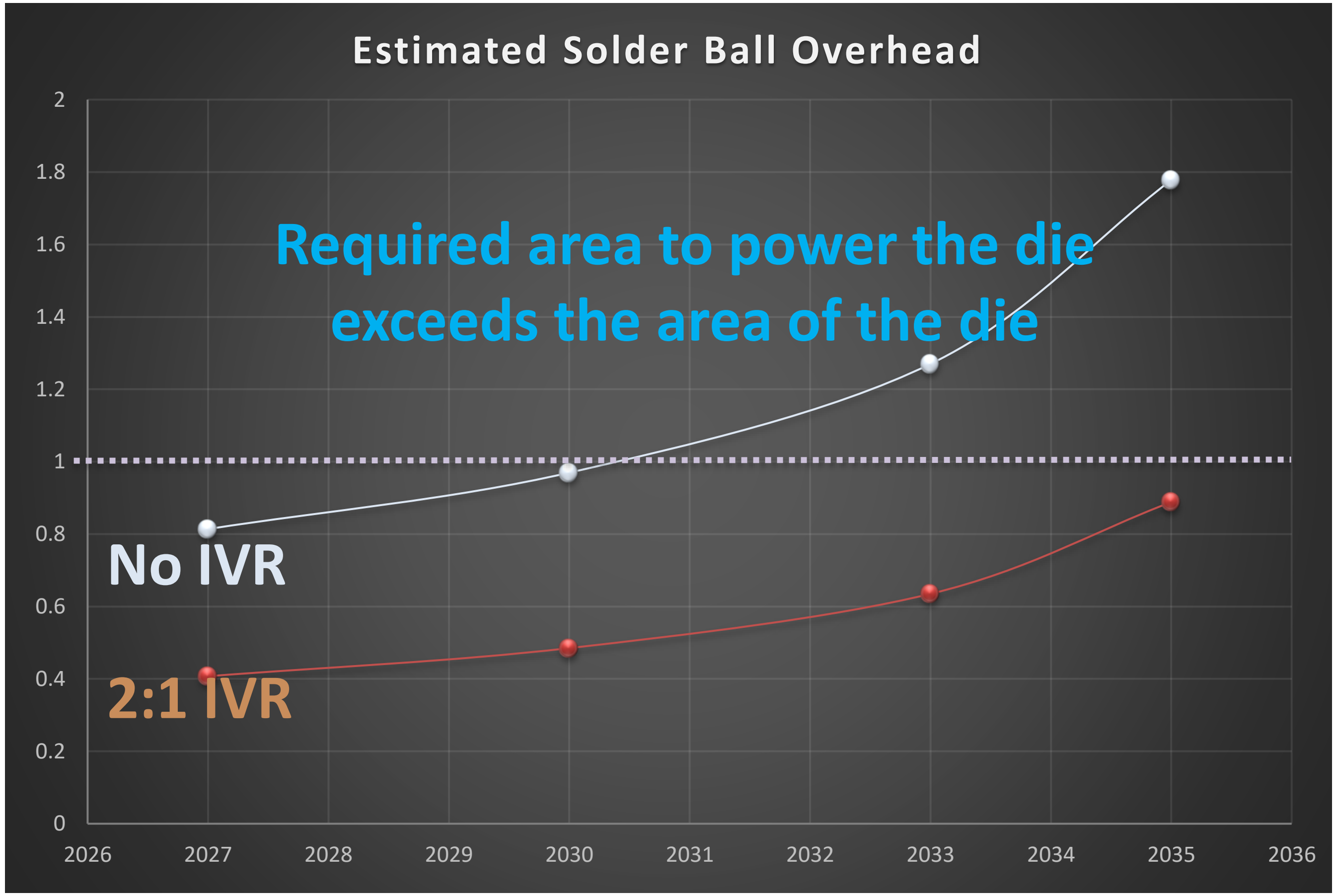
Reduce resistance of high current path



1.8V to 0.7V, 2.2x lower input current



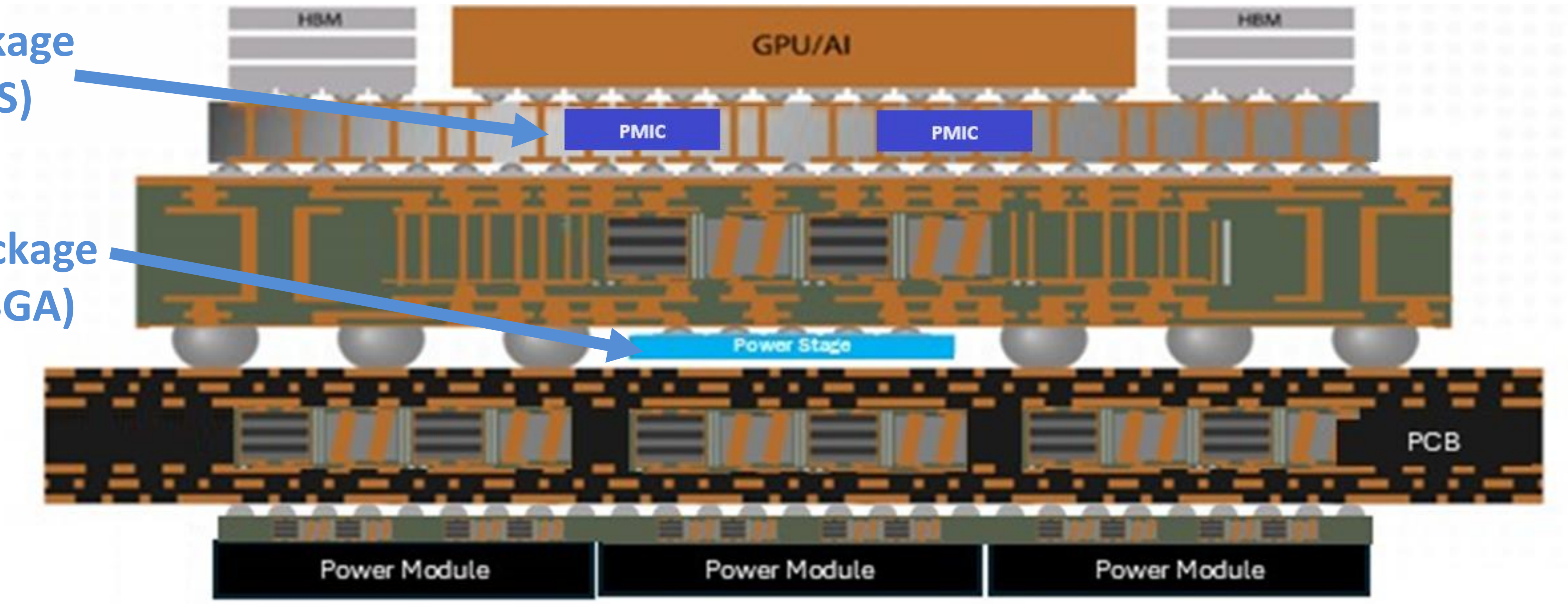
IVR Technology is a Must Have for Future AI Processors



Maximum Solder Ball Current is limited by Thermal Mechanical Stress

More Balls ➔ Larger Footprint ➔ Larger PDN Resistance

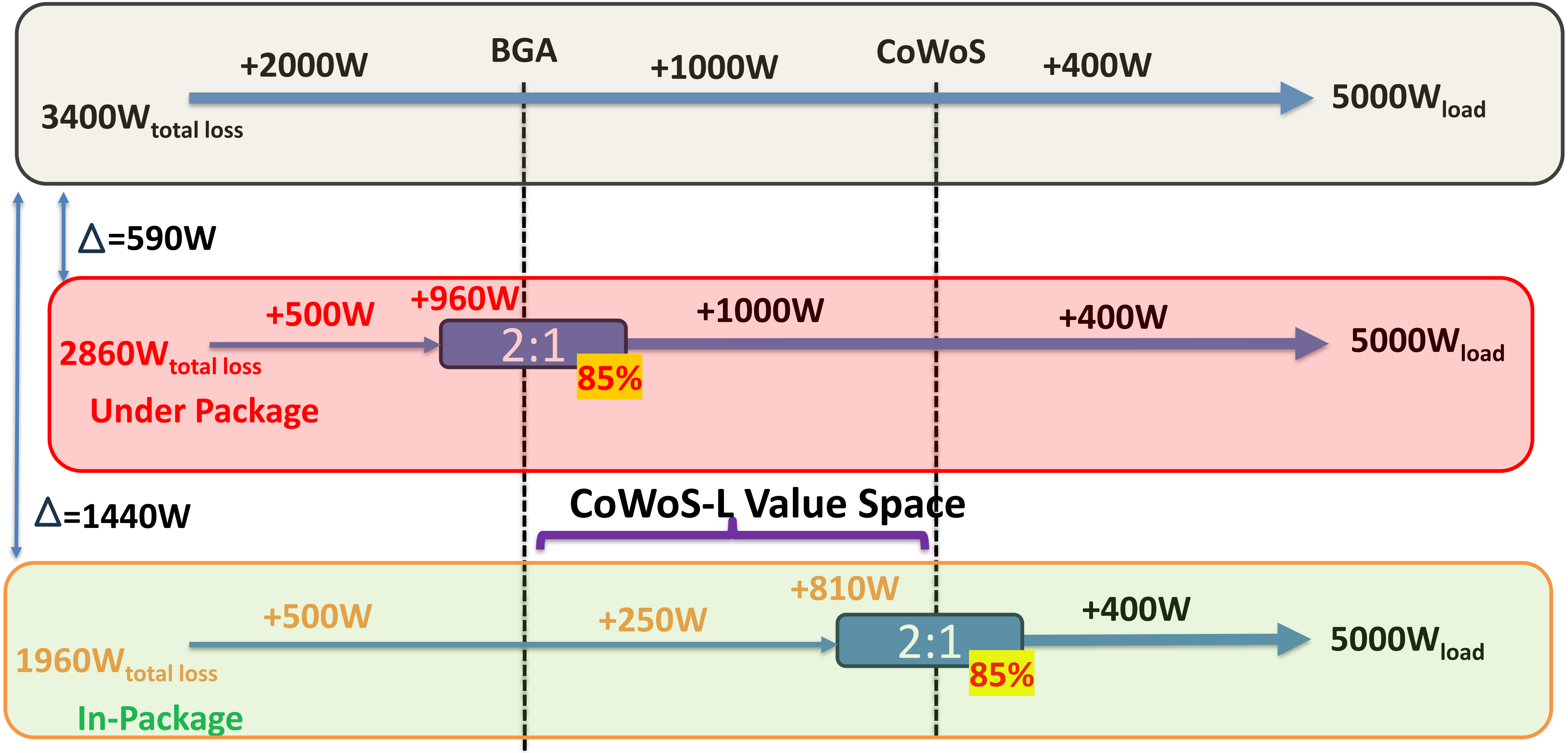
Vertical Stack-Up



In-Package
(CoWoS)

Under-Package
(Bottom BGA)

Why, now where



BGA

CoWoS

3400W$_{\text{total loss}}$

+2000W

+1000W

+400W

5000W$_{\text{load}}$

Δ=590W

Δ=1440W

2860W$_{\text{total loss}}$

Under Package

+500W

+960W

2:1

85%

+1000W

+400W

5000W$_{\text{load}}$

CoWoS-L Value Space

1960W$_{\text{total loss}}$

In-Package

+500W

+250W

+810W

2:1

85%

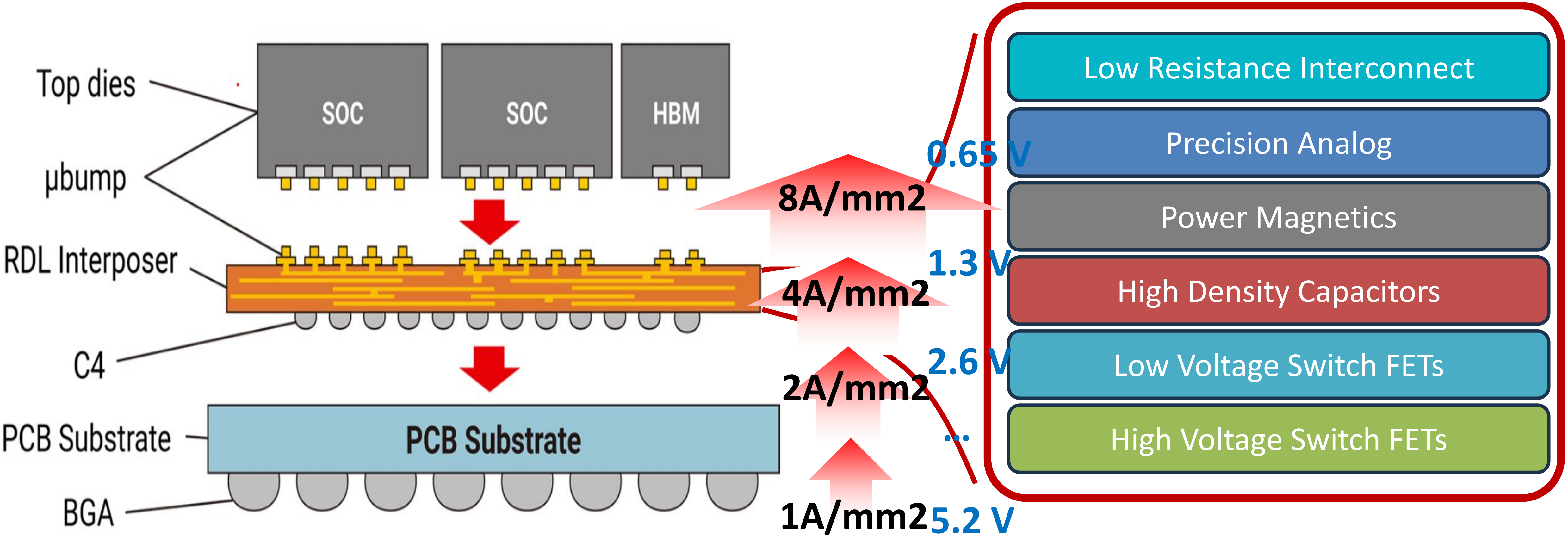
+400W

5000W$_{\text{load}}$

*Calculations are based on hypothetical 2:1 Regulator with 85% Efficiency system using estimated parasitics and losses from multiple sources

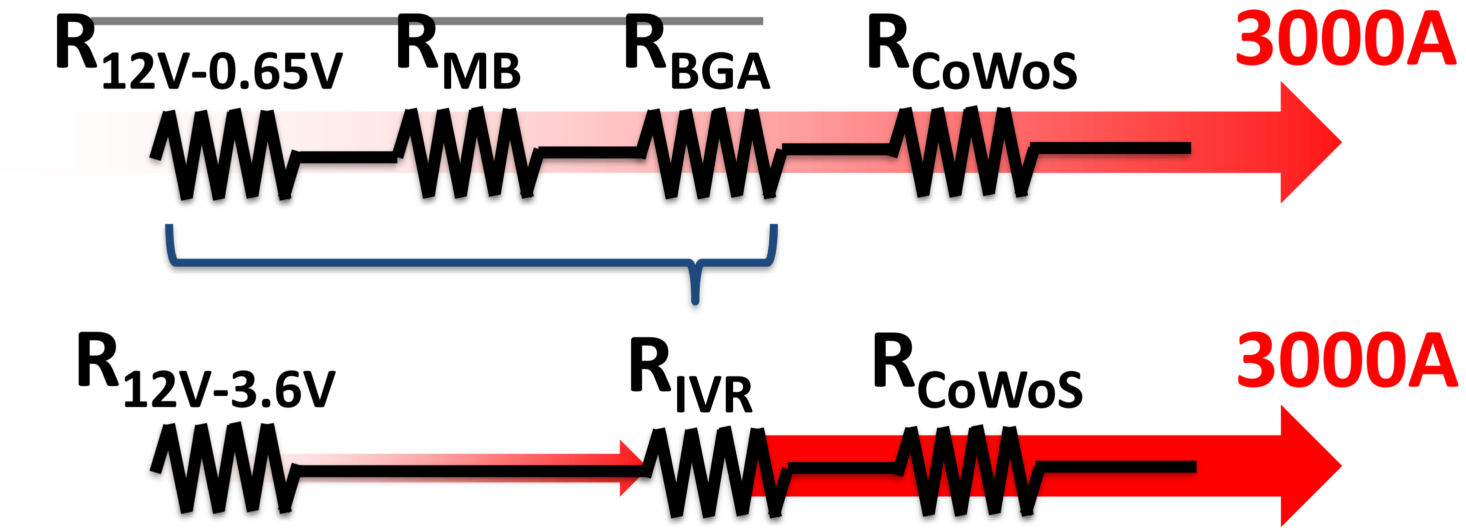
What Ingredients should be on the RoadMap

In-Package IVR Ingredients



- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- High Voltage Switch FETs

Full Load – Resistance Dominates Efficiency



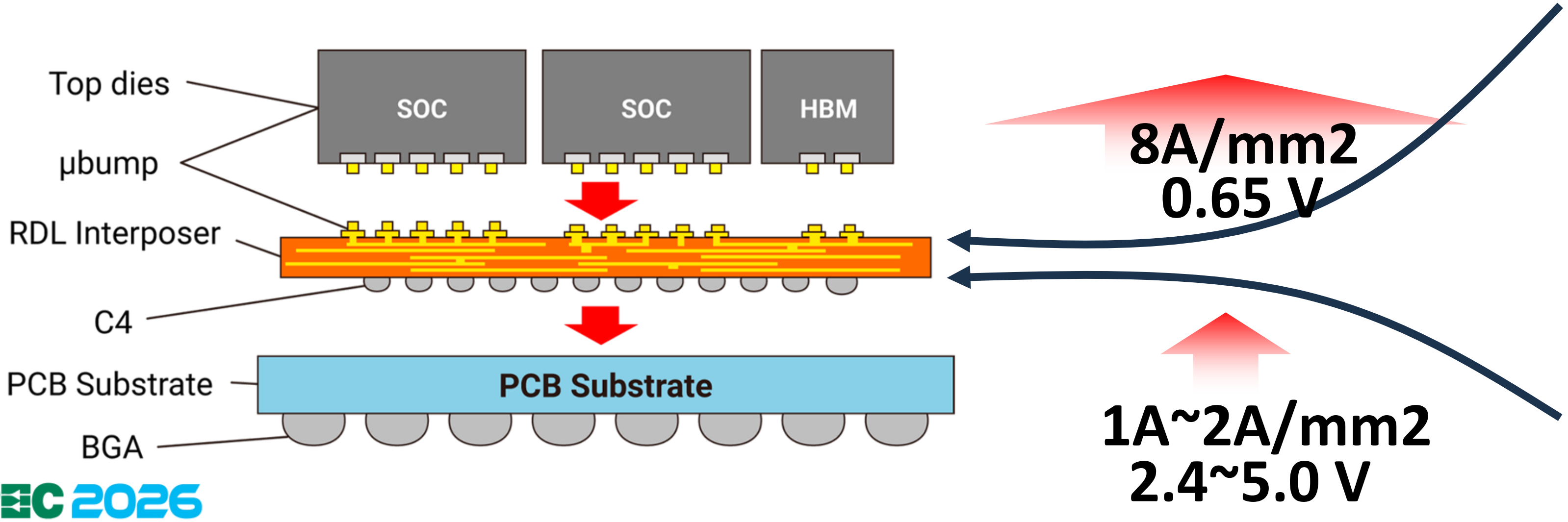
$R_{12V\text{-}0.65V}$ R_{MB} R_{BGA} R_{CoWoS} **3000A**

$R_{12V\text{-}3.6V}$ R_{IVR} R_{CoWoS} **3000A**

R_{IVR}

- **Magnetics**
  - Low DCR and ACR
- **Interconnect**
  - Resistance & EM Rules
- **Semiconductors**
  - Low Rdson and Coss

$R_{12V\text{-}3.6V} + R_{IVR} < R_{12V\text{-}3.6V} + R_{MB} + R_{BGA}$



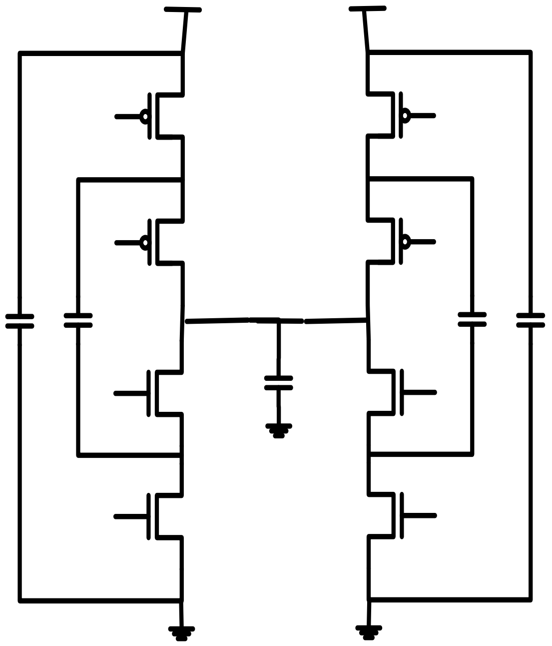
8A/mm2
0.65 V

1A~2A/mm2
2.4~5.0 V

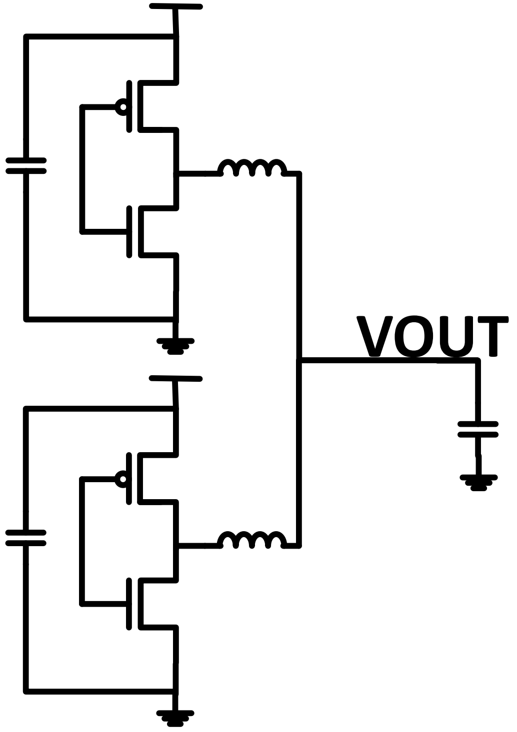
- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- High Voltage Switch FETs

Which Topology for 2:1

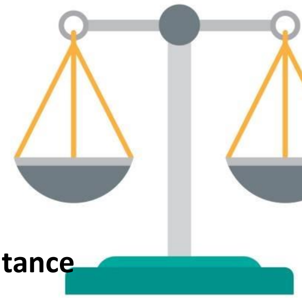
2:1 SwCap



2:1 Buck



Efficiency



SwCap

No magnetics
Discrete Regulation
Low Bandwidth
Requires >20x Capacitance

- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors ++
- Low Voltage Switch FETs
- High Voltage Switch FETs

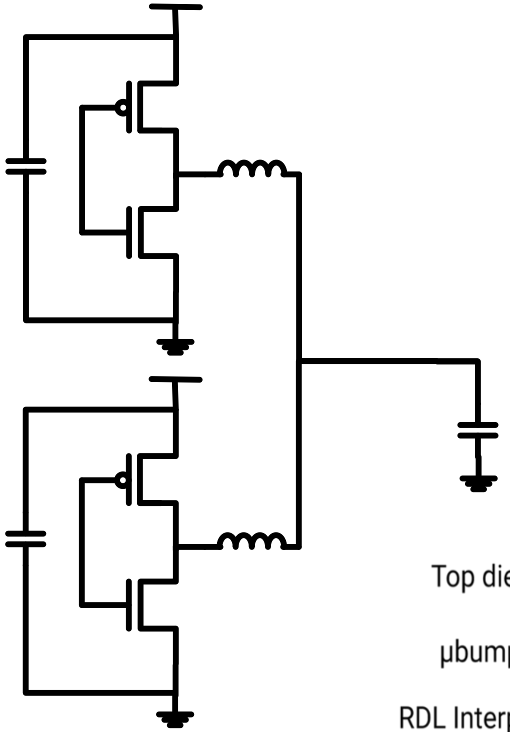
Buck

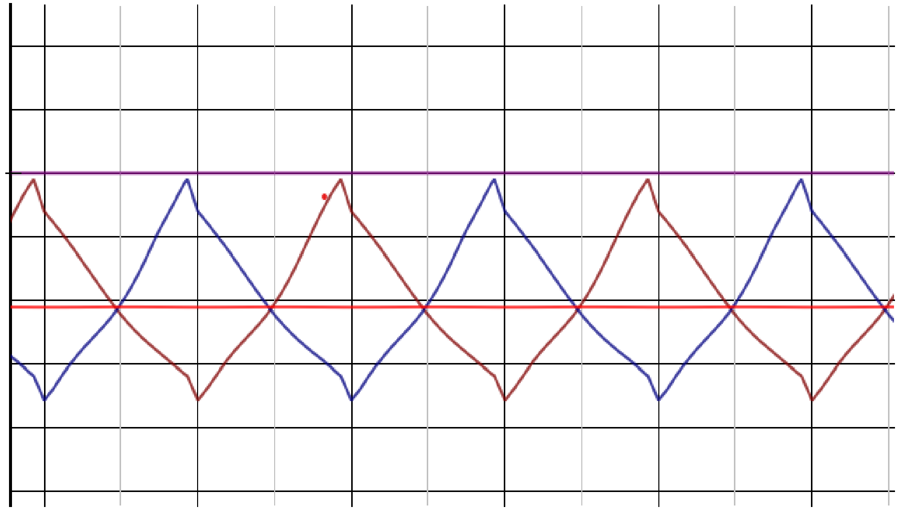
Lower ripple
Continuous Regulation
High Bandwidth
Current output

- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- High Voltage Switch FETs

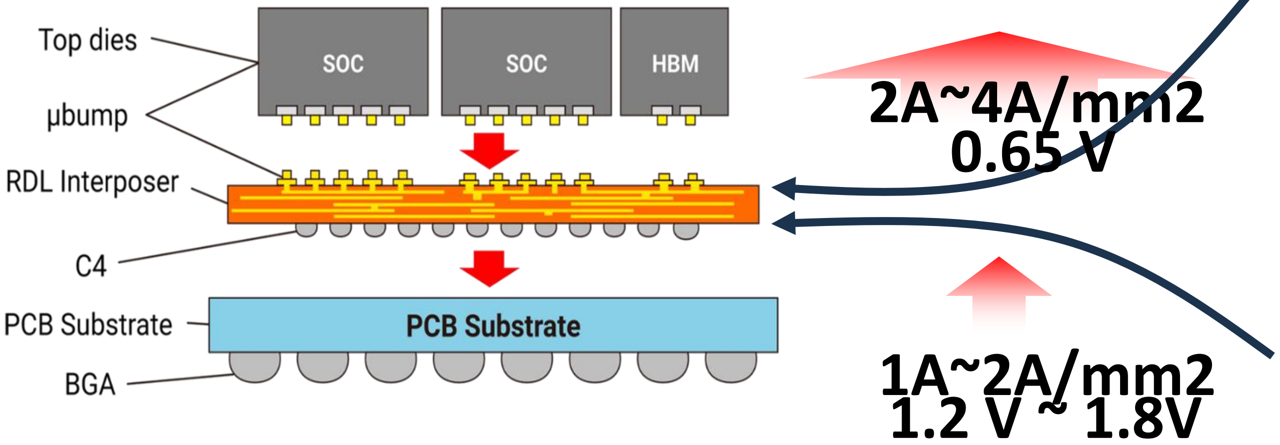
2:1 Switched Inductor

1.4V -> 0.7V





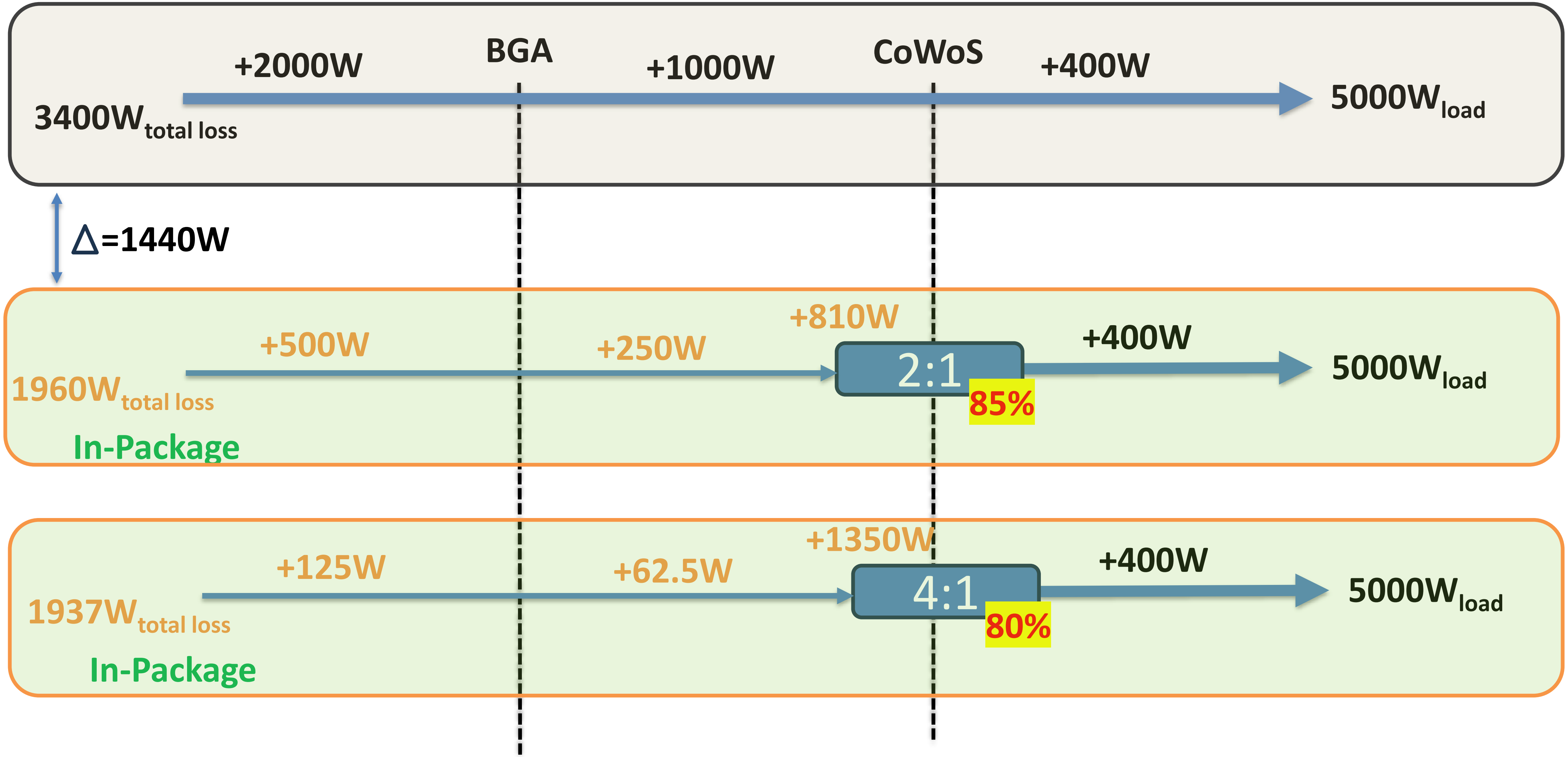
- **Efficiency: Good**
- **Regulator Losses < I^2R Losse**



In-Package IVR Ingredients

- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- ~~High Voltage Switch FETs~~

Why, now where



$3400W_{\text{total loss}}$

+2000W

BGA

+1000W

CoWoS

+400W

$5000W_{\text{load}}$

Δ=1440W

$1960W_{\text{total loss}}$

+500W

+250W

+810W

2:1

85%

+400W

$5000W_{\text{load}}$

In-Package

$1937W_{\text{total loss}}$

+125W

+62.5W

+1350W

4:1

80%

+400W

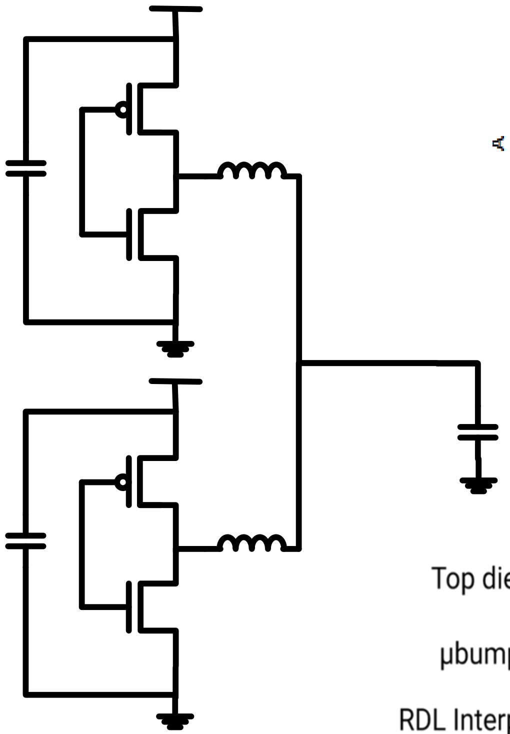
$5000W_{\text{load}}$

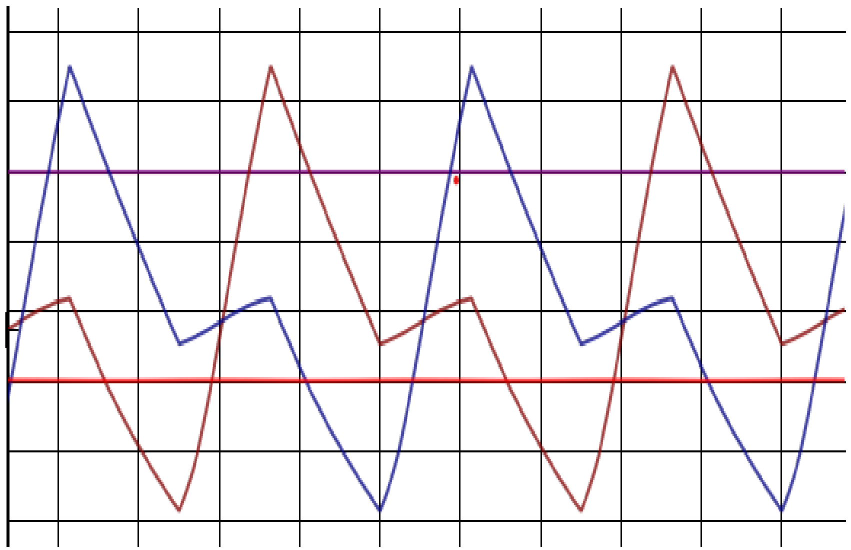
In-Package

*Calculations are based on hypothetical 2:1 Regulator with 85% Efficiency and 4:1 Regulator at 80% Efficiency system using estimated parasitics and losses from multiple sources

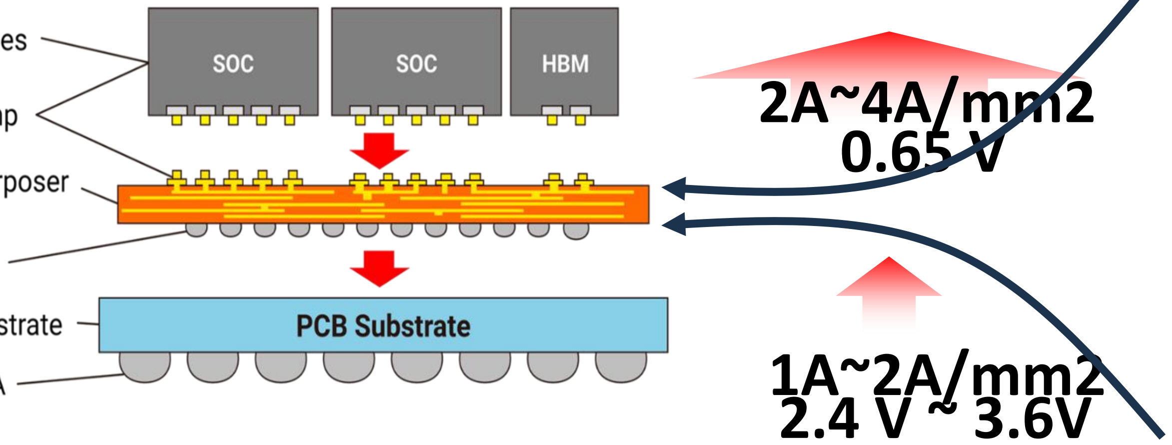
4:1 Switched Inductor

2.8V -> 0.7V





- **Relative Efficiency: Low**
- **Duty ratio drops from 0.5 to 0.25**
- **High Inductor current ripple**
- **Magnetic Stress**



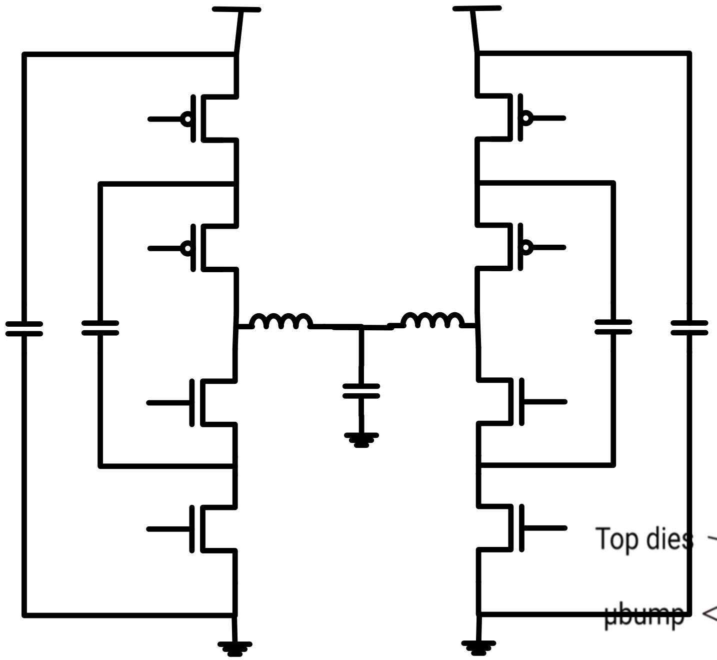
In-Package IVR Ingredients

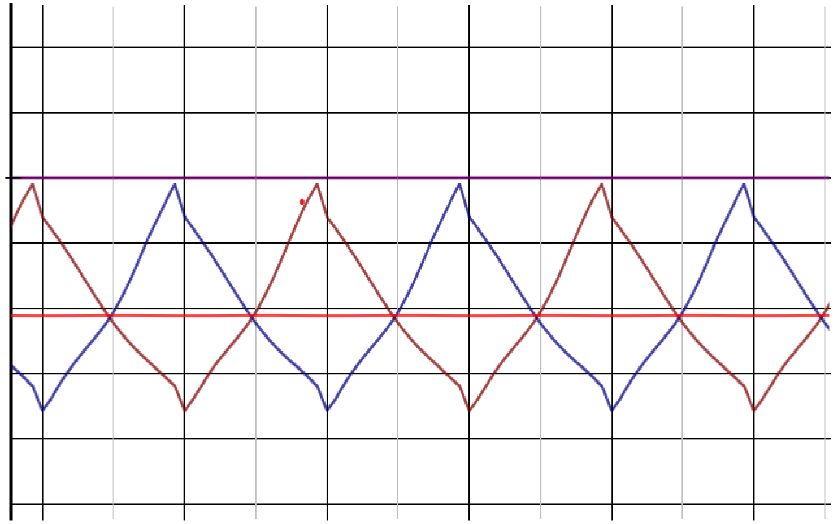
- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- ~~High Voltage Switch FETs~~

Requires High Voltage Transistors

4:1 – 3 Level Buck

2.8V -> 0.7V

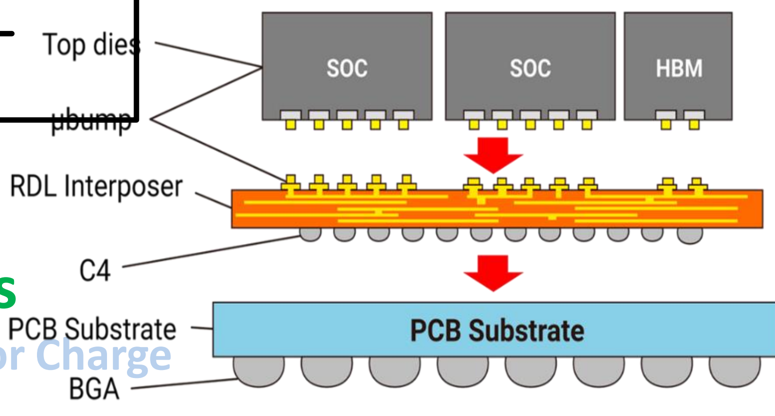




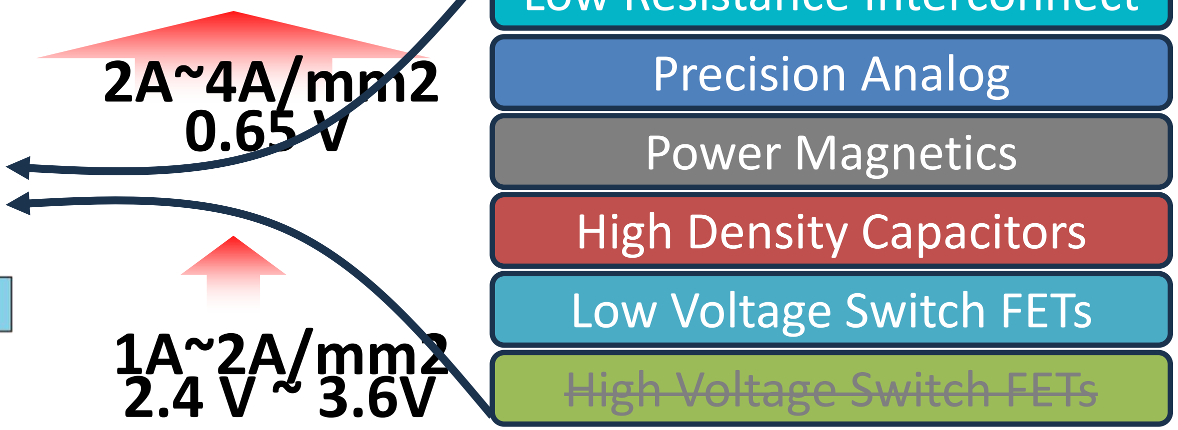
- **Efficiency: Good**
- **Regulator Losses < I^2R Losse**

Uses 1.8V Transistors

Circuits to Balance Capacitor Charge



In-Package IVR Ingredients

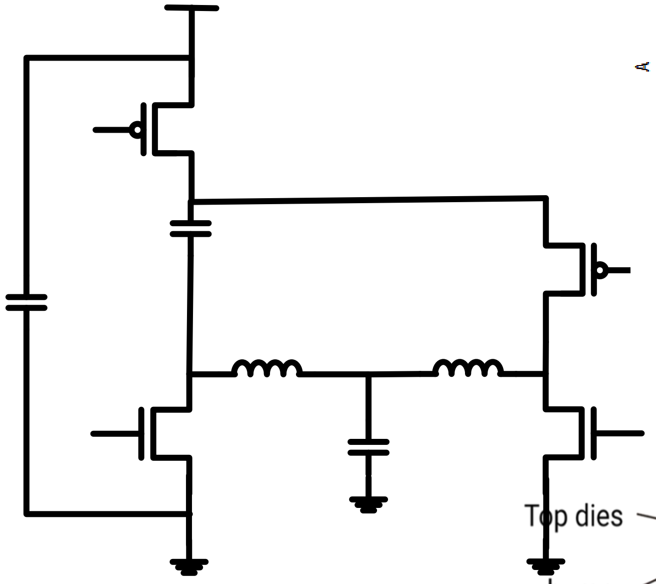


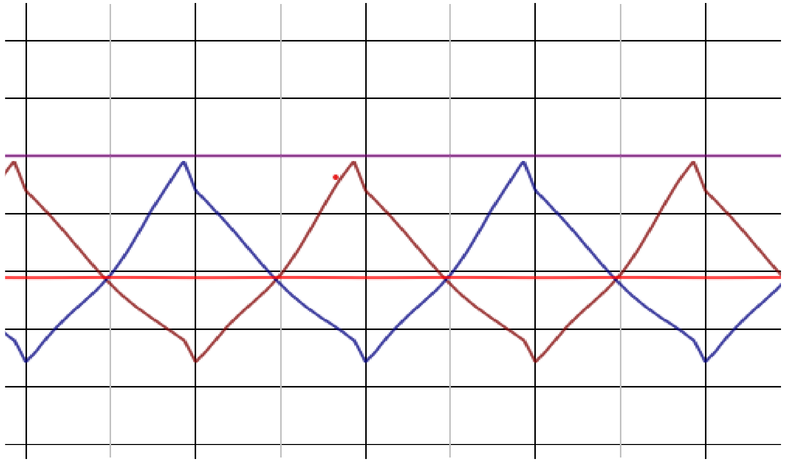
- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- ~~High Voltage Switch FETs~~

4:1 – Series Capacitor Buck

2.8V -> 0.7V

2-Level 2-Phase Buck

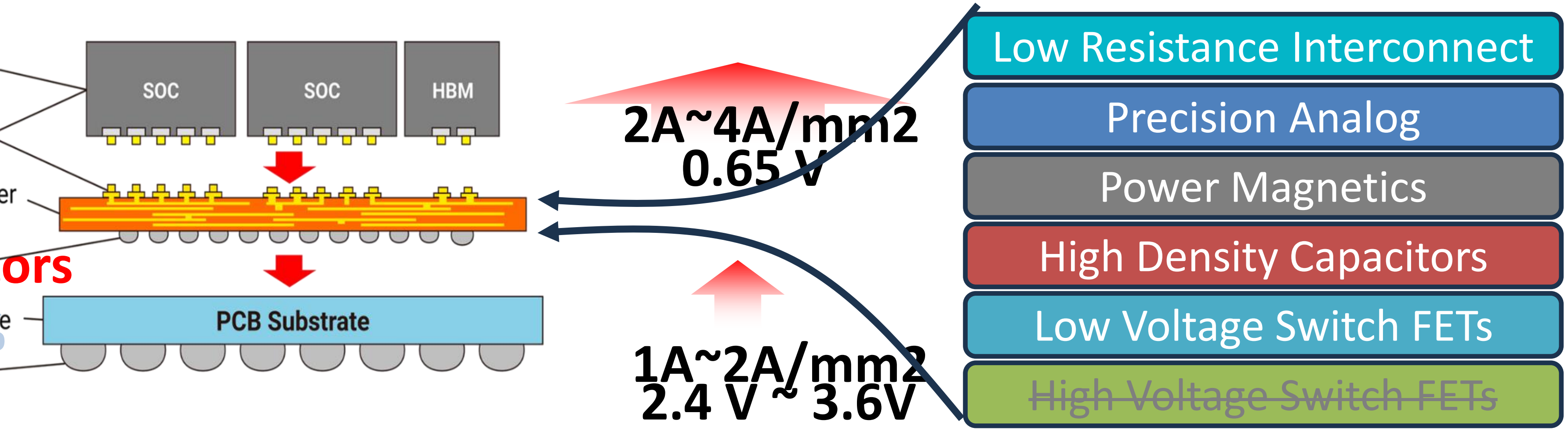




Same Inductor ripple same as 2:1 Buck

4:1 Efficiency: Better than 3-Level

In-Package IVR Ingredients



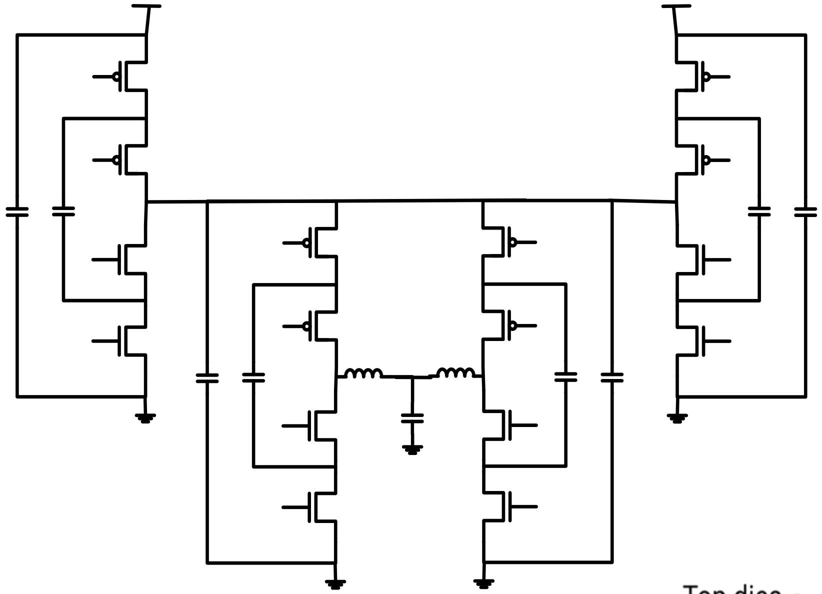
- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- ~~High Voltage Switch FETs~~

Requires >3.0V Transistors

Conversion Ratio < 50%

8:1 – Switch Cap + Switch Inductor

5.6V -> 0.7V

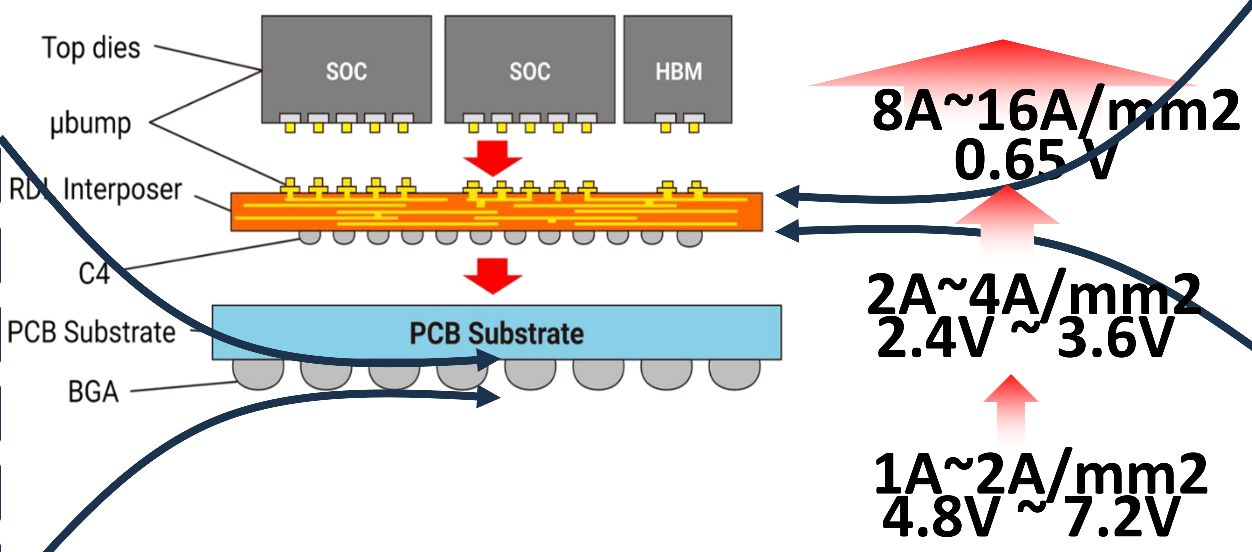


Switch Cap Stage operates Independently
Switch Cap Stage is Un-Regulated 2:1 Charge Pump
Same Inductor ripple as 2:1 Buck
Switch Cap Operates at 1/10 Buck Frequency

Current and Voltage Ripple same as 2:1 Buck
Maintains High Bandwidth Benefits of the Buck

Under-Package IVR Ingredients

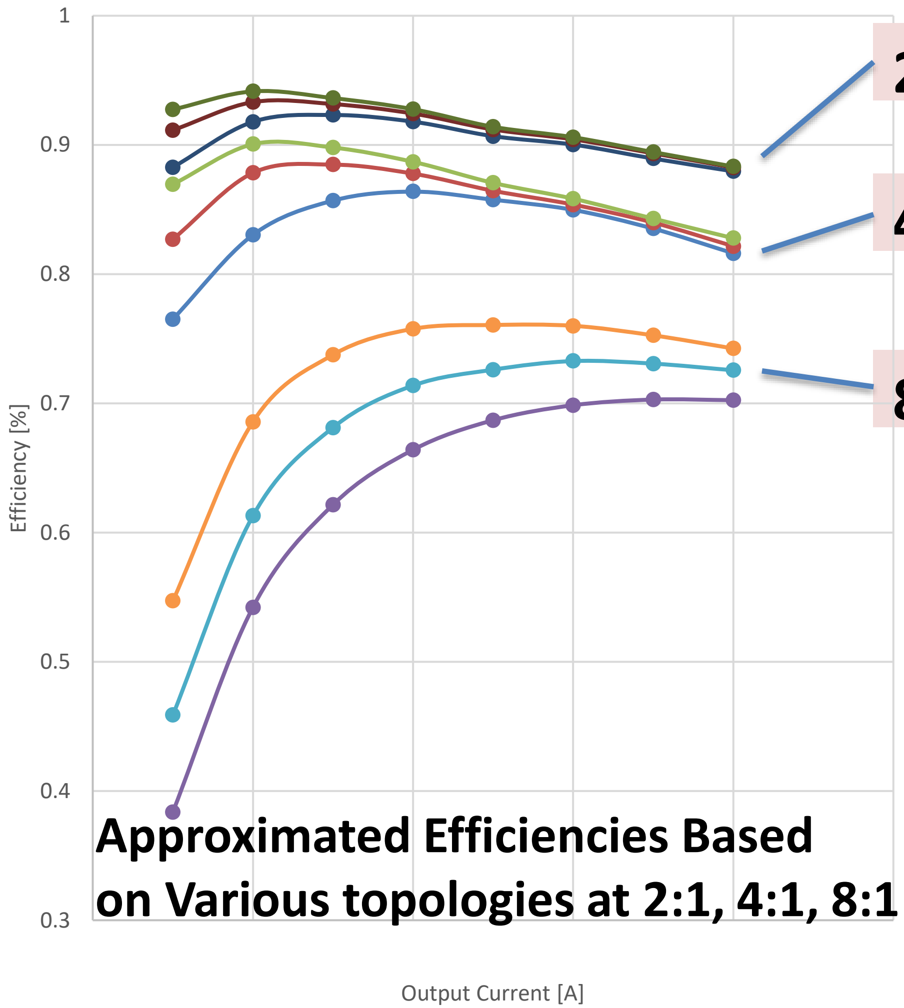
- Low Resistance Interconnect
- ~~Precision Analog~~
- ~~Power Magnetics~~
- High Density Capacitors
- ~~Low Voltage Switch FETs~~
- High Voltage Switch FETs



In-Package IVR Ingredients

- Low Resistance Interconnect
- Precision Analog
- Power Magnetics
- High Density Capacitors
- Low Voltage Switch FETs
- ~~High Voltage Switch FETs~~

Target Efficiency from 2:1 to 4:1 to 8:1



Approximated Efficiencies Based on Various topologies at 2:1, 4:1, 8:1

2:1 IVR ~ 85% efficiency → 1.8V to 0.65V IVR

I^2R and 4x Ball Count Benefits

5% drop

4:1 IVR ~ 80% efficiency → 3.6V to 0.65V IVR

16x Ball Count Benefits

10% drop

8:1 IVR ~ 70% efficiency → HV Capacitors and HV Switches

Single Location or Split Location

Efficiencies are based on estimated switching and conduction losses and are not representative of any particular implementation or solution

Summary

- Vertical power deliver provides a roadmap for scaling power deliver to match the scaling of computing
- In-Package Voltage Regulators benefits reducing the number of solder balls and lowering I^2R losses
- TSMC is providing a roadmap of future technologies to enable IVR implementations that match the industries needs.

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(Optional: Contact Information)